EXPERIMENTAL BENCHMARKING OF CVD GRAPHENE FOR MEMORY AND INTERCONNECT APPLICATIONS

A Dissertation
Presented to
The Academic Faculty

by

Ramy Nashed Bassely Said

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
August 2019

EXPERIMENTAL BENCHMARKING OF CVD GRAPHENE FOR MEMORY AND INTERCONNECT APPLICATIONS

Approved by:

Dr. Azad Naeemi, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Eric Vogel
School of Materials Science and Engineering
Georgia Institute of Technology

Dr. Muhannad Bakir
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Francky Catthoor
Electrical Engineering Department
Katholieke Universiteit Leuven

Dr. Jeffrey Davis
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: April 25th, 2019

To my Parents and my Wife

ACKNOWLEDGEMENTS

I am extremely grateful to my mother, who did not stop supporting me until her last day in this life. I can never forget her always-comforting words during the moments when I was down. She will always remain the symbol of sacrifice and pure love and giving for me. In fact, if there is one reason why I was able to make it to this point in my academic life, that would be HER.

I am also very thankful to my dad who taught me the meaning of hard work and always encouraged me to reach the utmost of my potential. His supporting words has always been the nurture of my self-confidence and belief that anything in this life is achievable through hard work and commitment.

I cannot thank my wife enough for being such a supportive person in good as well as bad times. I would like to thank her for patiently and happily tolerating my long working hours and her flexibility with our lifestyle that was sometimes highly unstable. I also would like to thank her for being such a selfless person who would always put my needs before hers.

I would like to thank my sister, who is also my lifetime friend, for always cheering me up with her cute sense of humor and kind heart. I am thankful to my father-, mother-, and sister-in-law for their continuous support.

I am extremely indebted to my advisor Prof. Azad Naeemi for guiding me through the arduous process of learning how to do research. He has always been very caring and supportive and would really put the benefit of his students first. I can not thank him

enough for standing by my side during my mom's illness and after she passed away and emphasizing that family comes first. Simply, I could not have hoped for a better advisor and I am honored to have worked with Prof. Naeemi.

I would like to thank Dr Francky Catthoor, Dr Zsolt Tokei, and Dr Inge Asselberghs for their generous invitation to conduct part of my PhD work at IMEC, Belgium and for their continuous support and very intellectual discussions and comments during my stay there.

I would like to thank my committee members for their time and support in the crafting of this work. I would like to extend a special thanks to Dr Eric Vogel who has been very generous to open his lab doors for me to learn the tricks of growing and transferring CVD graphene.

I am greatly thankful to Dr. Chenyun Pan whose simulation work gave a new dimension to this work and provided a more complete picture of the performance of graphene-based memory and interconnects. I would also like to thank Dr. Kevin Brenner, Chris Perini, and Xiangyu Wu for helping me build my fabrication skills and teaching me the tricks for graphene growth and fabrication.

Last but not least, I would like to thank my friends and colleagues in the Nanoelectronics Research Laboratory for their insightful discussions.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

The continuous increase in the 3D memory density required an increase in the height of the 3D stack. This, in turn, dictated an increase in the width of the memory hole that is accompanied by a reduction in the electric field inside the memory hole. To compensate for the reduced electric field, an increase in the programming voltage and/or programming time is required at the expense of higher power dissipation and/or slower memory operation. Furthermore, with the continuous scaling of feature size, interconnects become the dominating factor in determining the performance of electronic circuits due to increased RC delay of interconnects, increased crosstalk between nearby interconnect lines, increased dynamic power dissipation, and reliability issues due to electromigration.

In this thesis, we study CVD-grown graphene as a potential candidate for memory as well as electrical interconnects applications. Graphene can compensate for the reduced electric field in 3D memory devices while keeping the programming voltage sufficiently low by enhancing the electric field at its atomically thin, sharp edges. Furthermore, Graphene is considered a promising alternative to copper interconnects owing to its current carrying capability that can reach 10^8 A/cm^2 [1], ultrahigh intrinsic carrier mobility [2], and low resistivity [3]. Our Approach is outlined as follows:

- First, we extract the field enhancement factor (β) of CVD-grown single layer graphene (SLG) based on an MOS structure where we solve the contradiction in prior experiments that reported a field enhancement factor of few thousands but only 30-40% improvement in the write voltage of floating gate memory devices.

Based on this experimentally extracted value of β, we investigate the advantages of using CVD graphene as a floating gate layer in flash memory. We perform rigorous SPICE simulations for a 64-bit NAND flash string based on a 65nm predictive technology model. These simulations are used to quantify the advantage of using CVD graphene as the floating gate material, which enables unique tradeoffs in device operation.

- Second, we study CVD-grown SLG as a potential candidate for electrical interconnect applications. A simple two-step lithography process to fabricate high-mobility graphene devices is proposed. The extracted mobility is used to benchmark SLG against copper interconnects.
- Third, we propose an accurate method to determine the interlayer resistivity of top-contacted two-dimensional layered systems based on the direct measurement of the resistance at a mono-to-bi layer step and feeding the measured resistance to a distributed resistance model to extract the interlayer resistivity. The extracted values were used to analyze the performance of multilayer graphene (MLG) interconnects with different stacking orientations in terms of interconnect delay, energy dissipation, and energy-delay product.
- Fourth, we propose two different test structures from which high frequency circuit parameters such as interlayer capacitance, quantum capacitance, and kinetic inductance can be extracted, allowing for an accurate analysis of the frequency response in MLG interconnects.

CHAPTER 1. INTRODUCTION

Over the past fifty years, the microelectronics industry has grown at a very fast pace, becoming a trillion-dollar industry and finding its way into almost all the products of modern civilization. The main driving factor for microelectronics development is the scaling down of the feature size of the electronic building blocks, namely transistors and interconnects. Figure 1-1 [4] summarizes the development of the microelectronics business over the past 40 years. As the technology evolves, smaller feature sizes are attained (Figure 1-1a) which lead to the integration of more transistors per unit area (Figure 1-1b). This in turn brings the cost per transistor down (Figure 1-1c) leading to an increase in the worldwide semiconductor revenue (Figure 1-1d).

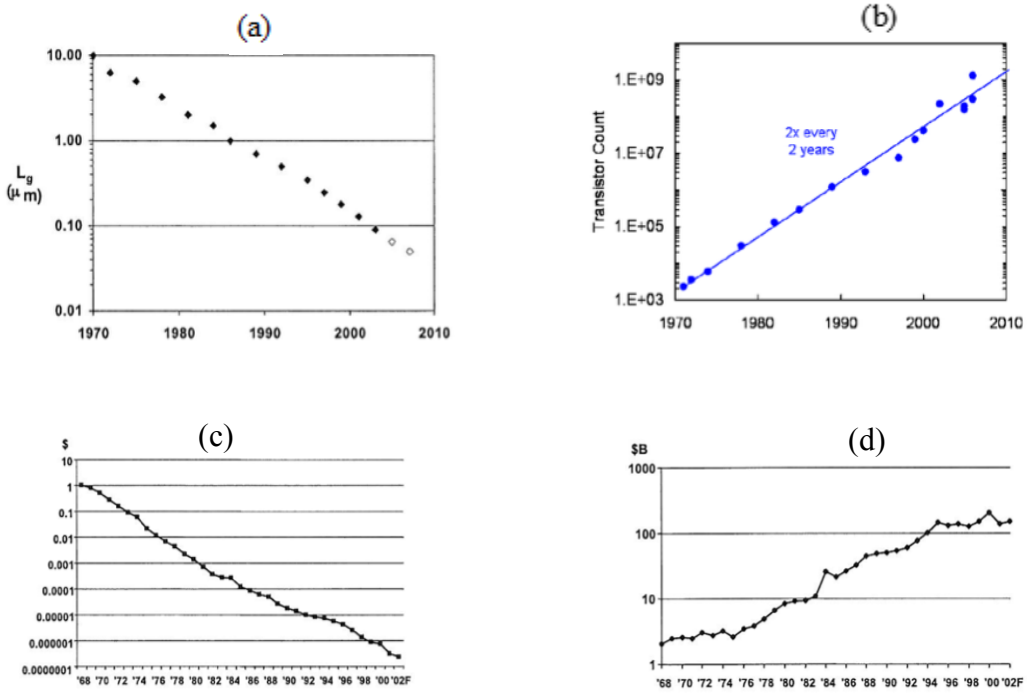


Figure 1-1: (a) Minimum Feature Size, (b) Transistor count trend for Intel processors, (c) Average transistor price per year, (d) Worldwide Semiconductor Revenue [4]

As the size of transistors shrinks, new technological barriers appear in the horizon that need to be addressed by engineers and scientists working in this field. For example, as both the oxide thickness and channel length get shorter, the control over the gate becomes very challenging. New solutions were proposed to circumvent this problem including the use of high-k materials for the gate instead of SiO_2 [5], double- [6] and triple-gate[7] structures. Nowadays, three-dimensional FinFET transistors are being used in all modern processors. However, it seems that CMOS transistors are approaching some fundamental limits especially as some device dimensions will only be a few atoms large at the sub-10nm technology nodes [8-10]. This imposes a gigantic problem to flash memory devices specifically, which are based on a floating-gate structure, since they require a tight gate control for their operation. Furthermore, the continuous scaling of transistors highlighted the delay problem in electrical interconnects, making them the bottleneck for achieving high-speed electronic devices.

Since its discovery in 2004 [3], graphene was considered a potential candidate in several electronic applications such as flexible electronics [11, 12], voltage amplifiers [13], digital logic [14, 15], digital non-volatile memory [16, 17], and electrical interconnects [1, 18-21], owing to its ultrahigh mobility, current-carrying capacity, large heat conductivity, and atomic thinness [1, 3, 21, 22]. In addition to its unique electrical and thermal properties, the rapid development of graphene fabrication from the lab-scale exfoliation technique [3] to large-scale roll-to-roll processing of graphene sheets of sizes approaching the meter scale [23, 24] has attracted many scientists and engineers to consider graphene as an alternative/complementary technology to the current CMOS technology. In the next sections, we will discuss the challenges of floating-gate memory

as well as electrical interconnects technologies in more details and show how graphene can potentially help overcome these challenges.

1.1 Justification of Research

1.1.1 Floating-Gate Memory Challenge

Since its innovation in 1987, non-volatile flash memory has become the most widely used memory technology, especially in portable devices, owing to its low power consumption, high packing density, and low cost [25, 26]. Floating gate (FG) flash memory structure is the current industry standard. It is comprised of a silicon channel substrate, a thin tunneling dielectric, a floating gate, a control dielectric, and a control gate. Figure 1-2a illustrates a schematic diagram for the floating gate flash memory. Logic state '0' is achieved by applying a large positive voltage to the control gate. This attracts the electrons in the substrate channel which, in turn, tunnel to the floating gate where they are retained, leading to a positive shift in the threshold voltage. When a small read voltage is applied to the control gate, the transistor will stay in the OFF state due to its large threshold voltage. On the other hand, logic state '1' is achieved by applying a negative voltage to the control gate which will push the electrons stored in the floating gate back to the substrate; hence decreasing the threshold voltage. When a small positive read voltage is applied to the control gate, the transistor will be turned ON due to the relatively small threshold voltage.

One of the most important performance metrics in floating gate flash memories is the gate-coupling ratio (GCR), which is the ratio of the voltage drop across the tunneling

dielectric to the total voltage across the channel and gate [27-29]. Figure 1-2b shows the equivalent circuit of a floating gate device. The GCR is given by:

$$GCR = \frac{C_{FG}}{C_S + C_D + C_B + C_{FG}} \quad (1\text{-}1),$$

where C_{FG} is the control gate to floating gate capacitance, C_S is the floating gate to source capacitance, C_D is the floating gate to drain capacitance, and C_B is the floating gate to body capacitance. The value of the GCR needs to be maximized to ensure efficient transfer of the program voltage to the FG, which ultimately controls the writing speed of the memory cell.

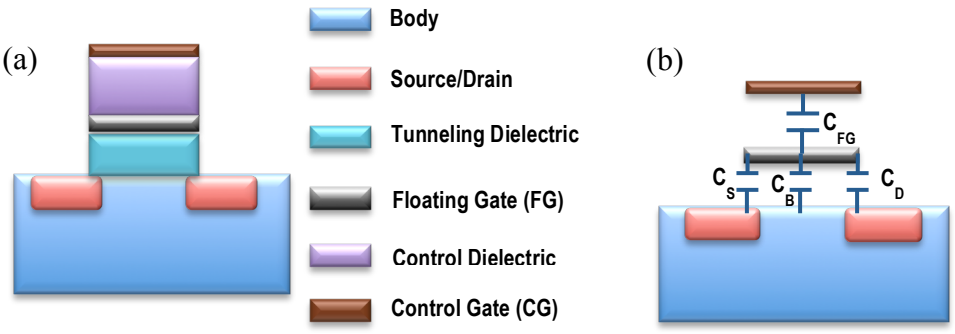


Figure 1-2: (a) Schematic diagram of the floating gate structure, (b) Equivalent circuit for the floating gate structure

With the continuous scaling of feature size in the current CMOS technology, the current flash memory technology is suffering from a constant decrease in GCR, keeping the writing speed of flash memory in the order of hundreds of microseconds whereas the data rate of modern microprocessors is in the order of nanoseconds [26]. Furthermore, the static power consumption increases with scaling due to increased subthreshold current. Also, the operational voltage of current memory elements is much higher than its

logical counterparts. As a result, memory components are the main bottleneck of present and future computing systems; hence, new materials/structures need to be explored to solve the aforementioned problems.

A simple remedy to the reduction of GCR can be deduced from Equation 1-1. In order to maximize the value of GCR, the capacitance between the floating gate and the control gate needs to be maximized. This can be achieved by wrapping the control gate around the floating gate, which increases the surface area and hence increases the capacitance [28]. The main drawback of this structure is that it requires much larger space compared to its planar counterpart and hence the packing density of the memory elements is relatively small [28]. Another way to increase the control gate to floating gate capacitance is to use a high-k dielectric as the control dielectric [29]. This allows for a high GCR value without sacrificing the area constraints. However, most high-k materials have small bandgaps and charge carriers can be injected from the control gate to the floating gate during the write operation; thus annihilating the electrons tunneling from the channel to the floating gate [28]. This leads to a relatively small increase in the threshold voltage and consequently a small operation window between logic '0' and '1' states. Furthermore, high-k materials with sufficiently large permittivity tend to have low breakdown field [28]. On the other hand, high-k materials with large bandgaps tend to have relatively small permittivity. Charge Trap (CT) flash memory is an alternative to the conventional floating gate structure, which employs silicon nitride as a charge trap layer that can store charges. It is based on the fact that silicon nitride contains intrinsic defects that can store charges. The early version of charge trap flash memory consisted of a silicon nitride layer sandwiched between two thin (2-3 nm) tunneling silicon oxide layers

[30, 31]. The main advantage of the charge trap structure is that the gate directly controls the channel, hence eliminating the GCR issue. Furthermore, because the charge is localized, the crosstalk to neighboring cells is minimal. On the other hand, since the tunnel oxide is too thin, the stored charges in the nitride layer can induce a sufficiently large electric field that can cause the substrate holes direct tunneling; therefore, partially annihilating the electrons stored in the nitride layer leading to poor data retention [16, 28].

As the size of the memory cell is scaled down to sub-20nm, 2D technology faced serious technological challenges because the number of electrons per memory cell decreased significantly such that a small number of charge loss/gain due to leakage/interface led to a dramatic shift in the threshold voltage, leading to endurance and data retention degradation as well as higher likelihood of program disturb [32]. This led to the development of 3D memory technology in which memory cells are stacked on top of each other, allowing for ultrahigh density memory [33, 34]. Toshiba introduced the first industry-scale 3D memory technology in 2007, known as Bit-Cost Scalable (BiCS) [35], followed by Terabit Cell Array Transistor (TCAT) technology introduced by Samsung in 2009 [36], then 3D Floating Gate technology presented by Hynix in 2010 [37], and the relatively new 3D XPoint developed by Intel and Micron around 2015 [38].

Figure 1-3 illustrates the basic concept of BiCS technology, which is based on Stack, Punch, Plug process [39]. Several conducting plates are first stacked on top of each other and separated by a dielectric layer. Then holes are punched in the structure and plugged with active materials to form the memory films. The memory cells are formed at the intersection between the conducting plates and the memory holes [39]. Some of the

3D memory technologies are based on FG structure while others are based on CT, however, the basic layout is very similar [35].

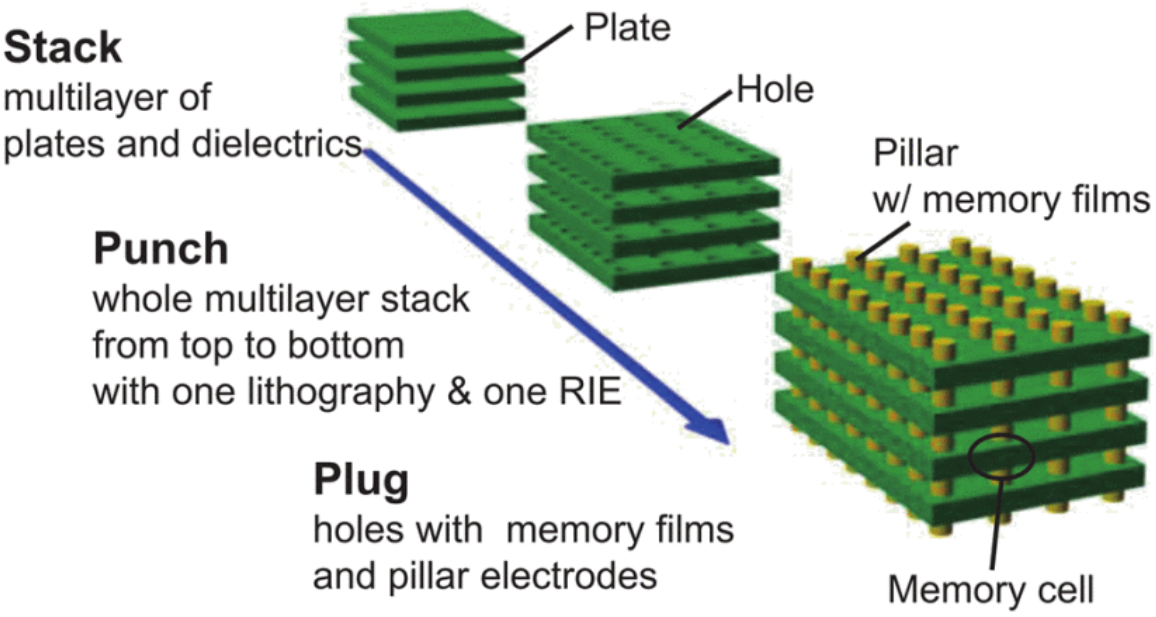


Figure 1-3: Basic concept of BiCS technology. It is based on stack, punch, plug process which represents the general concept of all 3D memory technologies [39].

In order to increase the memory density, more layers need to be stacked on top of each other. The main challenge facing most 3D technologies is to develop a Reactive-Ion-Etching (RIE) process that can uniformly etch the sidewalls of the memory hole [39]. This problem is illustrated in Figure 1-4 [40, 41] in which the memory hole suffers from a tapered profile since less etching ions reach the bottom of the memory hole compared to the top. This problem becomes more pronounced with increasing the height of the memory stack and may lead to a closed memory hole at the bottom, and consequently loss of electrical connection between the memory hole and the underlying electronic circuit driving the memory hole current, see Figure 1-4b [41]. One way to solve this problem is to increase the width of the memory hole to ensure that it is open all the way.

However, this reduces the electric field inside it and requires a higher program voltage, rendering it a non-appealing solution for low-power applications due to larger power consumption.

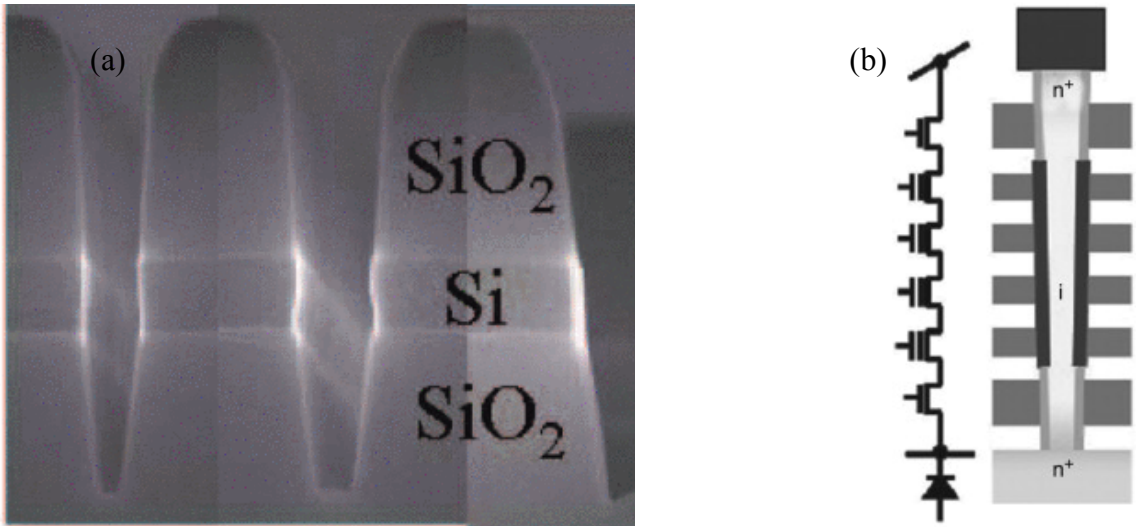


Figure 1-4: (a) SEM image illustrating the tapered structure in memory hole [40], (b) Schematic diagram showing that severe tapering of the memory hole may lead to loss of electrical connection to the underlying driver circuit, rendering the memory hole non-operational [41].

The tunneling current in floating gate devices is given by the Fowler-Nordheim relation [42]:

$$J_{FN} = a\,\beta^2\,E^2\,exp\left(-\frac{b}{\beta\,E}\right) \tag{1-2},$$

$$a = \frac{q^3}{16\,\pi^2\,h\,\varphi_b}, b = \frac{4}{3}\,\frac{\sqrt{2\,m_{ox}}}{q\,h}\,\varphi_b^{3/2}$$

Here, q is the electron charge, h is Planck's constant, m_{ox} is the effective mass of the electron in the tunneling dielectric, and φ_b is the potential barrier that the electrons must overcome to tunnel through the dielectric.

One important figure of merit for the FN tunneling current is the field enhancement factor, β. The value of β, which functions as a scalar multiple to the applied voltage, is dictated by a local field enhancement that stems from the physical geometry of the FG layer [43, 44]. At the device-level, increasing the value of β above unity corresponds to reductions in both the programming voltage and/or programming time, which can counteract the reduction of the electric field caused by the increased memory hole diameter in modern 3D memory technologies. This is especially interesting for low-dimensional carbon nanomaterials, with sharp edges and tunable work functions, and has led to both graphene and carbon nanotubes (CNTs) being exploited for field emission sources [45-47]. The atomically-thin and extremely sharp edges of graphene enhance the electric field which, in turn, enhances the value of β. Furthermore, while graphene struggles with defect-limited mobility in transistor and interconnect applications, such defects can play a positive role in further enhancing the field emission [47, 48].

Reported values of β from graphene sheets (both monolayers and multilayer composite films) can reach as high as 25,000 [49]. Eda *et al.* deposited a graphene-polystyrene composite on degenerately doped Si substrate and reported a β of 1200 [50]. Malesevic *et al.* grew vertically aligned few-layer CVD graphene on Ti and Si substrates using microwave plasma enhanced CVD and reported a β of 5000 and 7500 for Si and Ti,

respectively [51]. Palnitkar *et al.* studied the effect of graphene doping on β [49]. They prepared undoped, boron-doped, and nitrogen-doped graphene using arc discharge technique and deposited it on Si substrate using electrophoretic deposition. The extracted β values were 15740, 11879, and 25849 for undoped, boron-doped, and nitrogen-doped graphene, respectively. Nitrogen-doped graphene showed the highest β probably due to the upshift of Fermi energy which reduced the barrier that electrons need to overcome to tunnel to the Si substrate. Wu *et al.* [47] also used electrophoretic deposition to fabricate single-layer graphene films and reported a β of 3700. From (1-2), it can be seen that for β=1000, J_{FN} would be roughly multiplied by a factor of 10^6. This would cause a drastic decrease in the write voltage of the FG memory devices, namely, down to the μV range. However, Hong *et al.* reported graphene-based FG memory structures with a write voltage of around 7V [16]. Also, Hossain *et al.* reported a write voltage of 12V for a FG structure using carbon nanotubes as the floating gate and multilayer graphene as the channel [17]. Although the reported write voltage is lower than the current industry standard (~20V) [16], it is still much higher than the values predicted based on the β values previously mentioned. Furthermore, the reported β values were based on a structure in which graphene was deposited on a metal or degenerately doped Si substrate which might change the electrical properties of graphene, namely its Fermi energy and hence the barrier height. Therefore, a more accurate determination of β is required. We specifically solve the contradiction in prior experiments that reported a field enhancement factor of a few thousands but only a 30-40% improvement in the write voltage of floating gate memory devices by extracting the β value of graphene from an MOS structure. We then use the obtained experimental data to drive higher-level circuit simulations on 64-bit

NAND strings to identify performance improvements stemming from graphene integration.

1.1.2 Interconnect Challenge

Historically, the performance of electronic circuits was predominantly determined by the transistor resistance and capacitance values. However, as the feature size shrinks to the sub-micron scale, interconnects become the dominating factor in determining the performance of electronic circuits due to increased RC delay of interconnects, increased crosstalk between nearby interconnect lines, and increased dynamic power dissipation [52, 53]. The increased RC delay is partially attributed to the increased copper resistivity which increases with reducing the size due to surface and grain boundary scatterings and also surface roughness [54]. This increases the RC delay of the electronic circuits and hence reduces the operating frequency. Figure 1-5a [55] compares the gate delay with that of interconnect as a function of feature size. It is clear that as the feature size decreases, the gate delay monotonically decreases whereas the interconnect delay increases and becomes the dominant parameter in the total delay.

Also by shrinking the interconnect size, the current density increases leading to electromigration which in turn affects its reliability. Electromigration is a current-induced displacement of atoms, which leads to a partial removal of atoms from one side and building up of atoms in the other side leading to the formation of voids (open circuit) in the former case and short circuit in the latter as illustrated in Figure 1-5b [56]. The current density for electrical interconnects has already reached ~1.7 A/cm^2 in 2015, which is approaching the maximum current carrying capacity of copper [57].

Furthermore, employing 3D technology to ICs worsens the problem by allowing electromigration to happen at a much lower current density because of the high temperature generated by Joule heating [58]. Therefore, new materials with a higher breakdown current density need to be investigated.

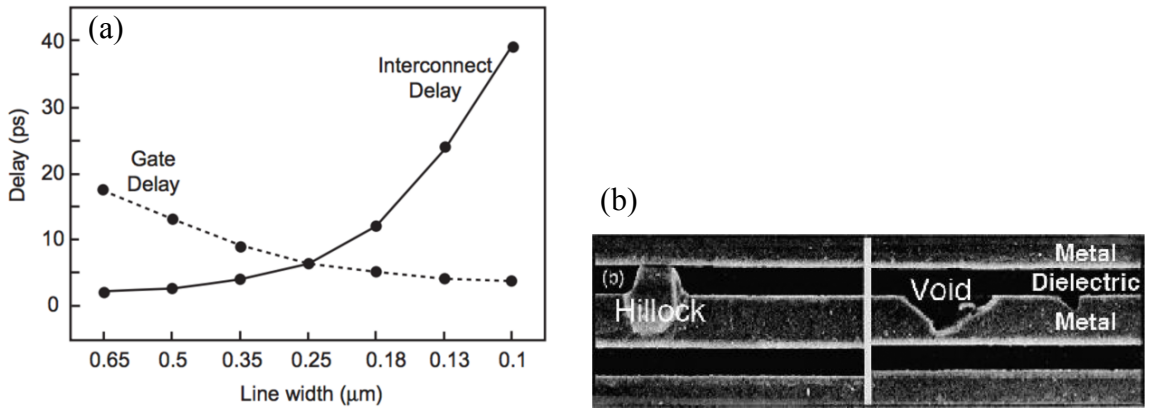


Figure 1-5: (a) Trends in transistor gate delay (switching time) and interconnect delay (propagation time for the Al/SiO_2 system) with integrated circuit fabrication technology. The cross over point represents the start of the "interconnection bottleneck", (b) Hillocks and voids induced by electromigration with high current density in a Cu interconnect

A great deal of research has been devoted to find more efficient materials for interconnects. Graphene is considered a promising material in this regard owing to its current carrying capability that can reach 10^8 A/cm^2 [1], ultrahigh intrinsic carrier mobility [2], and low resistivity [3]. Since the successful isolation of graphene from Highly Oriented Pyrolytic Graphite (HOPG) in 2004 [3], many efforts have been made to exploit its exceptional electrical properties [1, 18-21]. Unfortunately, most of these properties are washed out by fabrication-induced damage, making real-life graphene devices a poor reflection of their theoretical benchmarks. Chemical Vapor Deposition (CVD) is the most appealing fabrication method of graphene due to its scalability,

relatively low cost compared to epitaxial graphene, and compatibility with the current CMOS process technology. The main hurdle to commercialize CVD-grown graphene was the relatively low mobility, which was in the range of 2000-4000 cm^2/V.s. [14, 59-62]. This is still far from the theoretical phonon-limited mobility of graphene on SiO_2 (40,000 cm^2/V.s) [63]. In order to improve the mobility of graphene, the electric field imposed by the charged impurities in the SiO_2/Si substrate on the charge carriers flowing through graphene should be minimized. Furthermore, the graphene should be well anchored to the substrate to minimize any fabrication-related residuals at the graphene-substrate interface. We present a simple approach to fabricate high mobility CVD graphene devices using hydrogen silsesquioxane (HSQ) as a dielectric to immediately pin down the CVD graphene sheet, post-transfer. This pinning dielectric provides a two-fold benefit: (1) mechanically anchors and protects the graphene and (2) provides a screening medium for charged impurities. In securing the graphene, peripheral issues related to the poor adhesion of contact metals to the graphene surface and mechanical abrasion at the graphene-SiO_2 interface during agitation are addressed.

Multilayer graphene (MLG) can provide an even lower resistance and probably lower delay and energy-delay product compared to single layer graphene (SLG). This is because MLG provides more conduction paths compared to SLG and therefore has an overall lower resistance [64]. However, MLG has larger capacitance and therefore the number of graphene layers should be optimized to minimize the RC delay. Interlayer resistivity (ρ_c) is one of the most important intrinsic parameters affecting the performance of MLG interconnects as it was found that for a relatively small interlayer resistivity, electric current tends to redistribute itself among the different layers. [65] Additionally,

ρ_c affects the delay and energy-delay product. For the same number of layers, the delay increases with increasing ρ_c because the effective number of conduction channels is reduced.

For these reasons, it is important to understand the origin and accurately determine the value of ρ_c so that MLG interconnects can be optimized accordingly. Several theoretical and practical studies have been conducted to determine the value of the interlayer resistivity and compare it with the in-layer resistivity [66-72]. Wallace used tight binding method to study the interaction between adjacent layers in graphite [66]. He found that the interlayer resistivity depends on the exchange potential between the electrons in the adjacent layers. This in turn suggests that the interlayer resistivity depends on the overlap between the p_z orbitals in the adjacent layers. Therefore, interlayer resistivity should be greatly affected by stacking faults between adjacent layers since a large misorientation angle between adjacent layers would lead to a small overlap between the p_z orbitals and hence a relatively large ρ_c. This mechanism was also suggested by Uher and Sander [69] and Habib *et al.* [70] who also attributed large ρ_c value to the stacking faults between graphite layers. In fact, Habib *et al.* [70] showed that ρ_c monotonically increases by increasing the misorientation angle between adjacent layers in bilayer graphene. Other studies suggest that the large value of ρ_c stems from localized states along the c-axis of graphite [67]. A more recent study shows that ρ_c is affected by lattice defects that enhance the electronic coupling between the layers giving rise to a quasi-3D electronic spectrum with coherent transport along the c-axis [68]. Furthermore, it was shown that ρ_c is a function of the Fermi energy [70], which, in turn, is a function of doping.

Unfortunately, the reported values for interlayer resistivity vary by several orders of magnitude [67, 69, 73], which hampers the accurate modeling of MLG interconnects performance and can lead to misleading analyses. For example, Morgan and Uher [67] measured ρ_c to be as small as 1×10^{-3} Ω.m whereas Sui and Appenzeler [73] reported a value of 0.3 Ω.m, which is two orders of magnitude larger. Furthermore, Uher and Sander [69] showed that ρ_c changed by one order of magnitude between the different samples that they measured. The disagreement between the different reported values can be partially attributed to the quality of the samples and possibly due to the difference in the extent of stacking faults of adjacent graphene layers [67, 69, 71]. Also, some of the measured graphite crystals were not exactly rectangular in the xy plane, so the dimensions used to calculate ρ_c were not exact [72]. However, one important factor affecting this disagreement is the method by which the interlayer resistivity is measured. All the aforementioned experiments used four-probe measurement technique to extract the resistance where they put two contacts on each side of a thick graphite sample and apply a vertical electric field across its thickness. This vertical electric field was shown to modify the band structure of graphite [74] which can potentially alter the effective mass of electrons in the c-direction and, in turn, affect the value of ρ_c. This suggests that more accurate measurements of ρ_c need to be done in order to accurately analyze MLG interconnects. Furthermore, measurements should be done on graphene samples rather than graphite because their band structures and their effective masses are different, which would lead to different ρ_c. It is worth mentioning that Kim *et al.* [75], measured the interlayer resistivity of twisted bilayer graphene (BLG) by fabricating a graphene cross junction where two exfoliated monolayer graphene strips are transferred on top of each

other and the resistance is measured at the overlap region. They extracted an interlayer resistivity of ~2000 Ω.cm at 280K. Although their study provided a very good insight about the range of interlayer resistivity in exfoliated BLG, it did not provide a full picture of the variation of interlayer resistivity as a function of twist angle as well as the number of graphene layers. In this regards, we propose an accurate method of measuring the interlayer resistivity of top-contacted MLG. We systematically study how interlayer resistivity evolves with increasing the number of graphene layers (up to four layers) as well as the twist angle between them. Four-probe technique was implemented on a graphene ribbon, which has more number of layers on one side compared to the other side. Current is injected from the side that has more graphene layers to that with fewer layers. This ensures that the charge carriers cross between the layers allowing for the measurement of interlayer resistivity. The voltage is measured across the interface between the two graphene regions and the measurements are fed into a distributed resistance model to extract the interlayer resistivity. We compare the interlayer resistivity of twisted CVD graphene to that of AB-stacked graphene as a function of carrier concentration. It is worth mentioning that this method is generic and can be applied to any two-dimensional layered structures such as metal dichalcogenides.

1.2 Organization of The Thesis

This work begins by discussing some of the technological barriers that hinder the further scaling of feature size of micro/nano-electronic devices. Specifically, the challenges that arise with further scaling of 2D NAND flash memory and how 3D NAND provides a way to obtain ultrahigh density memory are discussed. Also the structure of 3D NAND and the problems that arise with its further scaling are discussed. In addition,

RC delay as well as electromigration problems facing current electrical interconnects are reviewed. Graphene is presented as a candidate to alleviate current challenges facing both memory and interconnect industries.

In Chapter 2, we discuss the introduction of graphene as a floating gate in 2D NAND floating gate flash memories due to the field enhancement capabilities of graphene [16, 26, 43, 50, 51, 76] which can lead to higher speed and/or low power memory arrays. We specifically try to address the contradiction in prior experiments that reported a field enhancement factor of few thousands but only 30-40% improvement in the write voltage of graphene-based floating gate memory devices. Towards this end, we experimentally benchmark 2D graphene sheets in a floating gate architecture and use the experimental data to drive circuit-level simulation on a mature 65nm non-volatile memory (NVM) technology, 64-bit 2D NAND strings. The field enhancement factor, at a barrier height of 3.1 eV is shown to be 2.06 with a standard device-to-device deviation of 0.33. This modest value explains the contradiction in prior experiments. The role of this enhancement factor is to expand the operational design window for G-NAND and enable improved programming time and/or programming voltage down to 10ns and 5V, respectively, at a 65nm process node. We restrict our analysis to 2D NAND due to the complex fabrication process of 3D memory; however, as mentioned earlier, this analysis can be extended to 3D memory since they both share the same building block (Floating Gate or Charge Trap structures).

Chapter 3 investigates graphene-based electrical interconnects. A simple two-step process to fabricate high mobility single layer CVD graphene is reported where a layer of Hydrogen Silsesquioxane (HSQ) is deposited on top of graphene right after the transfer

step. The advantage of HSQ is two-fold: (1) mechanically anchors and protects the graphene leading to minimal impurities at the graphene/substrate interface and a better adhesion of graphene and metal contacts to the substrate, and (2) provides a screening medium for charged impurities in the substrate leading to enhanced carrier mobility in graphene. The fabricated devices show mobilities up to ~9,500 $cm^2/V.s$ which is twice the average mobility values reported so far and among the highest recorded mobilities [59-62, 77].

The analysis of graphene interconnects is expanded in Chapter 4 where AB-stacked as well as twisted-multilayer graphene interconnects are considered. In Chapter 3 it was shown that even with the achieved high mobility, the energy-delay product of single layer graphene interconnects is still larger than that of Cu. Using multilayer graphene (MLG) can provide a lower resistance and probably lower energy-delay product compared to SLG because MLG provides more conduction paths compared to SLG and therefore has an overall lower resistance [64]. To determine the resistance of MLG, the interlayer resistivity between the graphene layers should be accurately determined. In this chapter an accurate method to measure the interlayer resistivity of top-contacted AB-stacked and twisted CVD graphene is proposed based on the direct measurement of the resistance at a mono-to-bi layer step and feeding the measured resistance to a distributed resistance model to extract the interlayer resistivity. This method is generic and can be applied to other two-dimensional layered systems such as metal dichalcogenides. The results show that the interlayer resistivity of AB-stacked CVD grown bilayer graphene is in the range of 50-140 Ω.m, which is three orders of magnitude greater than some of the previously reported values for AB-stacked graphite. On the other hand, twisted bilayer

graphene shows an interlayer resistivity as low as 6 Ω.m and it decreases monotonically with increasing the twist angle. Furthermore, the interlayer resistivity decreases with increasing the number of graphene layers for both AB-stacked and twisted graphene. This opens the path to further studying twisted MLG as a good candidate for electrical interconnect applications.

Chapter 5 concludes the work done in this thesis and provides directions for future work. Two different test structures are proposed from which high frequency circuit parameters such as interlayer capacitance, quantum capacitance, and kinetic inductance can be extracted, allowing for an accurate analysis of the frequency response in MLG interconnects. In the microstrip structure, the measured impedance was dominated by the large graphene resistance and/or metal/graphene contact resistance, whereas in the coplanar waveguide structure the measured impedance was dominated by the pad input capacitance. In order to be able to measure the high frequency circuit parameters of graphene, shorter graphene microstrips might be used that would have smaller resistance. Also, the contact area between graphene and the metal pad might need to be increased to reduce the contact resistance. For the coplanar waveguide structure, the distance between the signal and ground pads might need to be increased to reduce the value of the input capacitance.

CHAPTER 2. GRAPHENE-BASED FLOATING GATE FLASH MEMORY

Graphene is considered a promising material for modern non-volatile memory devices by virtue of its extremely high mobility [78], which may lead to faster operation time; its ultra-thin one-atom thickness, which may lead to more compact integration; and its low capacitance, which would lead to lower power consumption [16, 26]. This intrigued many researchers to explore the plausibility of using graphene in the state of the art, as well as, several emerging memory technologies. For example, Zheng *et al.* [79] demonstrated a graphene-ferroelectric hybrid memory structure where the binary information is represented by the high and low resistance states of graphene caused by switching the polarization of the ferroelectric thin film which changes the graphene's doping level. Unfortunately, these devices suffer from a low On/OFF ratio due to the gapless nature of graphene [26]. Furthermore, electrically-induced nanogaps in graphene can be utilized to produce a highly resistive state which complements the natural low resistive state in graphene, making graphene a potential material for resistive memory [80]. The low resistive state can be recovered by applying unipolar voltage stress or pulses. Although this structure provides a compact footprint, the achieved writing speed is rather slow (~100 ms) [80]. Graphene/metal interface can also be used to realize a resistive memory structure [81]. When an intrinsic graphene sheet comes in contact with a metal that has a similar work function as graphene, a large conduction barrier is developed at the graphene/metal interface due to the zero density of states of graphene at the Dirac point; resulting in a highly resistive state. On the other hand, when the graphene

sheet is electrostatically doped, a strong Coulombic interaction occurs between the metal and graphene leading to a low resistive state. Fabricating a high quality intrinsic graphene is the main hurdle against realizing high performance resistive memory based on graphene/metal interface structure due to the electron-hole puddles in graphene [82] as well as charged impurities [83] from the underlying substrate.

Besides being a promising candidate for emerging memory devices, graphene can also be employed in floating gate (FG) memory structure, which is mainstream memory technology. As mentioned earlier, the size of the memory holes in 3D memory technologies is increasing with increasing the height of the memory stack. This decreases the electric field inside the memory hole and hence a larger control voltage needs to be applied to the memory cells, which, in turn, increases the power consumption. Graphene can potentially alleviate this problem by enhancing the local electric field at its sharp edges [30-32], which multiplies the effective FG voltage by a field enhancement factor, β, eliminating the need to increase CG voltage.

In the next section, we explain the origin of electric field enhancement in graphene and discuss the early attempts to experimentally extract the field enhancement factor in graphene. After that we examine the validity of using Fowler-Nordheim equation (Equation 1-1) to describe the field emission from the graphene surface and discuss a modified FN equation [84] which has been derived to calculate the field emission in 2D systems. Then we discuss the discrepancy between previous experiments that reported a field enhancement factor of few thousands but only 30-40% improvement in the write voltage of FG memory and provide an accurate method to extract β, based on an MOS structure. We also compare the extracted β values from the traditional as well as

modified-FN equations to determine the reason behind the overestimated, previously reported values. This experimental data is then used to drive higher-level circuit simulations on 64-bit NAND strings to identify performance improvements stemming from graphene integration. These simulations were performed by Dr. Chenyun Pan.

2.1 Field Enhancement in Graphene-Based Floating Gate (FG) Structure

The atomically-thin and extremely sharp edges of graphene are the main reason behind the enhanced electric field from its surface, as illustrated in Figure 2-1 [85]. For a strip capacitor, the fringing electric field lines cause a non-uniform charge distribution along the strip where the charges are accumulated at the edges of the strip, as shown in Figure 2-1b [85, 86]. Several researchers have previously reported a large increase in carrier concentration at the edges of graphene [85, 87]. Although this phenomenon occurs in all strip capacitors as long as there is an appreciable fringing electric field, the electric field enhancement at the edges of the strip is more pronounced in case of graphene because the charges are concentrated on atomically thin edges which leads to very concentrated electric field lines and therefore, a very large electric field. Furthermore, the presence of sp3-hybridized bonds at graphene edges creates localized states which could possibly reduce the barrier for electron emission [31].

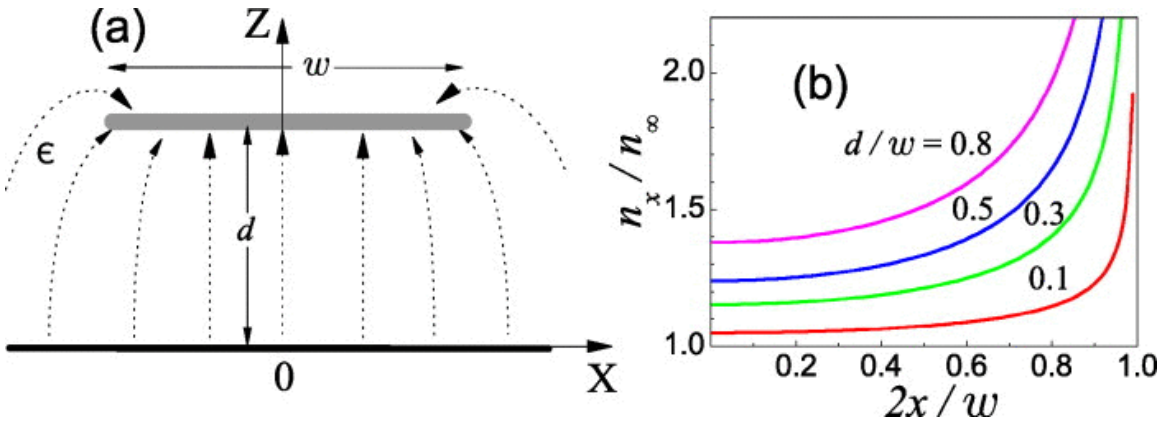


Figure 2-1: (a) Cross-section of a graphene strip of width w placed at the distance d over a gate. Dashed arrows show the field distribution under the applied gate voltage Vg. (b) Planar distribution of the carrier concentration, n_x, normalized to the concentration n_∞ (n_∞ is the concentration induced by V_g in an infinite homogeneous structure, $w \rightarrow \infty$).

Several reports have tried to experimentally determine the value of β [47, 49-51]. Eda *et al.* [50] deposited a graphene-polystyrene composite on degenerately doped Si substrate and achieved a β of 1200. Malesevic *et al.* [51] grew vertically aligned few-layer CVD graphene on Ti and Si substrates using microwave plasma enhanced CVD and reported β values of 5000 and 7500 for Si and Ti, respectively. Palnitkar *et al.* [49] studied the effect of graphene doping on β. They prepared undoped, boron-doped, and nitrogen-doped graphene using arc discharge technique and deposited it on Si substrate using electrophoretic deposition. The extracted β values were 15740, 11879, and 25849 for undoped, boron-doped, and nitrogen-doped graphene, respectively. Nitrogen-doped graphene showed the highest β probably due to the upshift of Fermi energy [49], which reduced the barrier that electrons need to overcome to tunnel to the Si substrate. Wu *et al.* [47] also used electrophoretic deposition to fabricate single-layer graphene films and reported a β of 3700.

The value of β is extracted from the Fowler-Nordheim (FN) model, which is the most widely used model for electron emission off a metal surface under a strong applied electric field [30-34]. For a traditional bulk material, the FN model relates the tunneling current density, J_{FN}, to the applied electric field, E, through (1-2), which is repeated here for convenience:

$$J_{FN} = a\,\beta^2\,E^2\,exp\left(-\frac{b}{\beta\,E}\right)$$

$$a = \frac{q^3}{16\,\pi^2\,h\,\varphi_b}, b = \frac{4}{3}\,\frac{\sqrt{2\,m_{ox}}}{q\,h}\,\varphi_b^{3/2}$$

Although almost all previous reports on graphene field emission used the aforementioned equation to estimate the value of β [47, 49-51, 76], the underlying assumptions leading to Equation 1-2 do not apply to 2D materials, which may lead to an inaccurate extraction of β. First, field emission in traditional bulk materials is not sensitive to direction of emission whereas in thin 2D materials the field emission can be divided into two types: (i) edge field emission (EFE) and (ii) surface field emission (SFE), as shown in Figure 2-2 [84]. Second, Equation 1-2 assumes a parabolic energy dispersion of the field emission material, which is an incorrect assumption in monolayer graphene as well as twisted few-layer graphene as they have a linear energy dispersion [84, 88, 89]. This could be one of the reasons behind the extremely large extracted β values and yet the modest improvement in graphene-based floating gate memory devices. A more accurate variation of the traditional FN equation was recently proposed by Ang *et al.* [84] which takes into account the non-parabolic nature of graphene band structure as

well as the sensitivity to emission direction. The modified FN-equation for 2D materials with linear energy dispersion is given by [84]:

$$J_{FN} = a\, exp\left(-\frac{b}{\beta\, E}\right) \qquad (2\text{-}1),$$

where a and b are the same constants as those in Equation 1-2 and β is the field enhancement factor. It is worth mentioning that the previously reported β values were based on a structure in which graphene was deposited on a metal or degenerately doped Si substrate which might change the electrical properties of graphene, namely its Fermi energy and hence the barrier height [36]. This can also lead to an inaccurate determination of β and is possibly another reason for the overestimated β values that were previously reported.

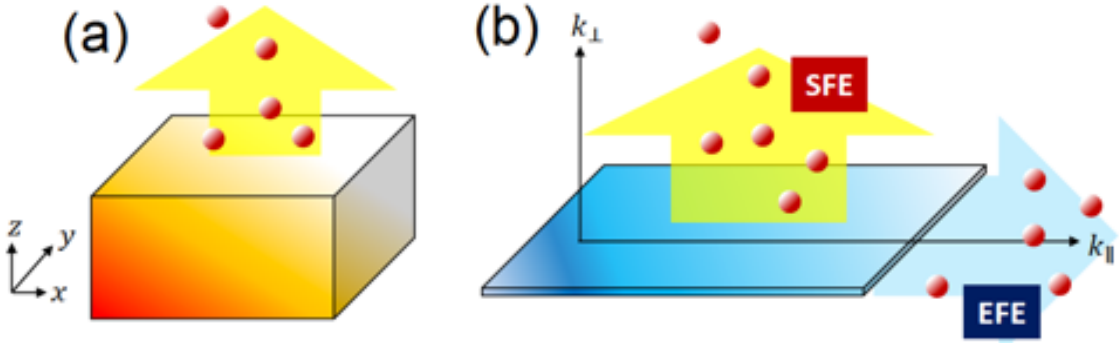


Figure 2-2: Electron emission from (a) three-dimensional bulk; and (b) two-dimensional plane. For emission from 2D plane, two emission configurations are possible, i.e. edge field emission (EFE) and surface field emission (SFE).

2.2 Fabrication Process for Graphene-Based MOS Structure

The field enhancement factor for CVD graphene sheets was extracted by fabricating MOS devices. The fabrication process flow is summarized in Figure 2-3. First, a 5nm SiO_2 tunnel oxide is thermally grown on top of a degenerately doped Si substrate (resistivity of ~0.001 Ω-cm) by placing the substrate in a quartz furnace and passing O_2 gas for 2 hours at 750°C. Second, a single-layer graphene sheet was grown and transferred onto the tunnel oxide layer using the process described in [90]. The quality of the transferred graphene was verified using Raman spectroscopy and is shown in Figure 2-4. The G band, which occurs around 1587 cm^{-1}, corresponds to optical phonons around Γ-point of the Brillouin zone whereas the 2D peak, occurring around 2680 cm^{-1}, corresponds to the double resonance process of optical phonons around K-point. As can be seen in Figure 2-4, the ratio of the 2D to G peaks is around 2, which is the indicator of monolayer graphene. The peak occurring around 2300 cm^{-1} is due to the SiO_2/Si substrate. 100×100μm^2 graphene devices were patterned using a JEOL JBX-9300FS electron beam lithography (EBL) with a dose of 600$\mu C/cm^2$ and a 35nm layer of 2% Hydrogen Silsesquioxane (HSQ) as resist. After exposure, the sample was developed in MF-319 and the pattern was transferred onto the graphene sheet using a 10s reactive ion etch (RIE) process with an O_2 plasma at 25W. Next, 70x70 μm^2 vias were patterned on HSQ using a second EBL step with a dose of 700$\mu C/cm^2$ and Poly(methyl methacrylate) (PMMA) as resist. The vias were then formed using a 5s wet etch in 1:1 Buffered Oxide Etchant (BOE) made from six parts of NH_4, and one part of HF. Here we opened vias in the HSQ resist instead of stripping it since HSQ was shown to improve the charge carrier mobility in graphene as well as mechanically pin the graphene sheet on the

substrate, leading to a better contact [78]. The remaining PMMA is then stripped by placing the sample in Acetone for 30 minutes. It is worth mentioning here that ZEP resist should be avoided in this step since it reacts with BOE and damages the fabricated EBL pattern.

Adjacent to each device, a reference device was fabricated where the graphene sheet had been etched away (in the first EBL step) as to provide a direct comparison between β with and without graphene. As such, the reference devices consisted of Pd directly contacting the SiO_2 tunneling dielectric. The graphene devices as well as the reference devices are fabricated by spin-coating 500nm of ZEP520A resist at a speed of 2000rpm for 60 seconds and using an EBL dose of 350μC/cm^2. The sample is developed in Amyl Acetate bath for 2 minutes followed by a 2-minute IPA bath. 80nm thick Pd pads are deposited using e-beam evaporation followed by a liftoff process in 1165 for 6 hours. The ground pads (second terminal of the devices) are then fabricated by etching the exposed SiO_2 using reactive ion etching under CHF_3 gas flow for 30 seconds. A final EBL step is employed to pattern the ground pads using ZEP520A under the same conditions mentioned earlier. A schematic 3D view of the devices is shown in Figure 2-3b.

Electrical testing of the devices was immediately carried out (post-metallization) under a vacuum of $1x10^{-4}$Torr at room temperature using a Lakeshore CPX probe station. A sweep of DC voltage from 0-12V was applied to the device using 2ms pulses to minimize charge trapping and hysteresis [91]. The tunnel current through the device was monitored.

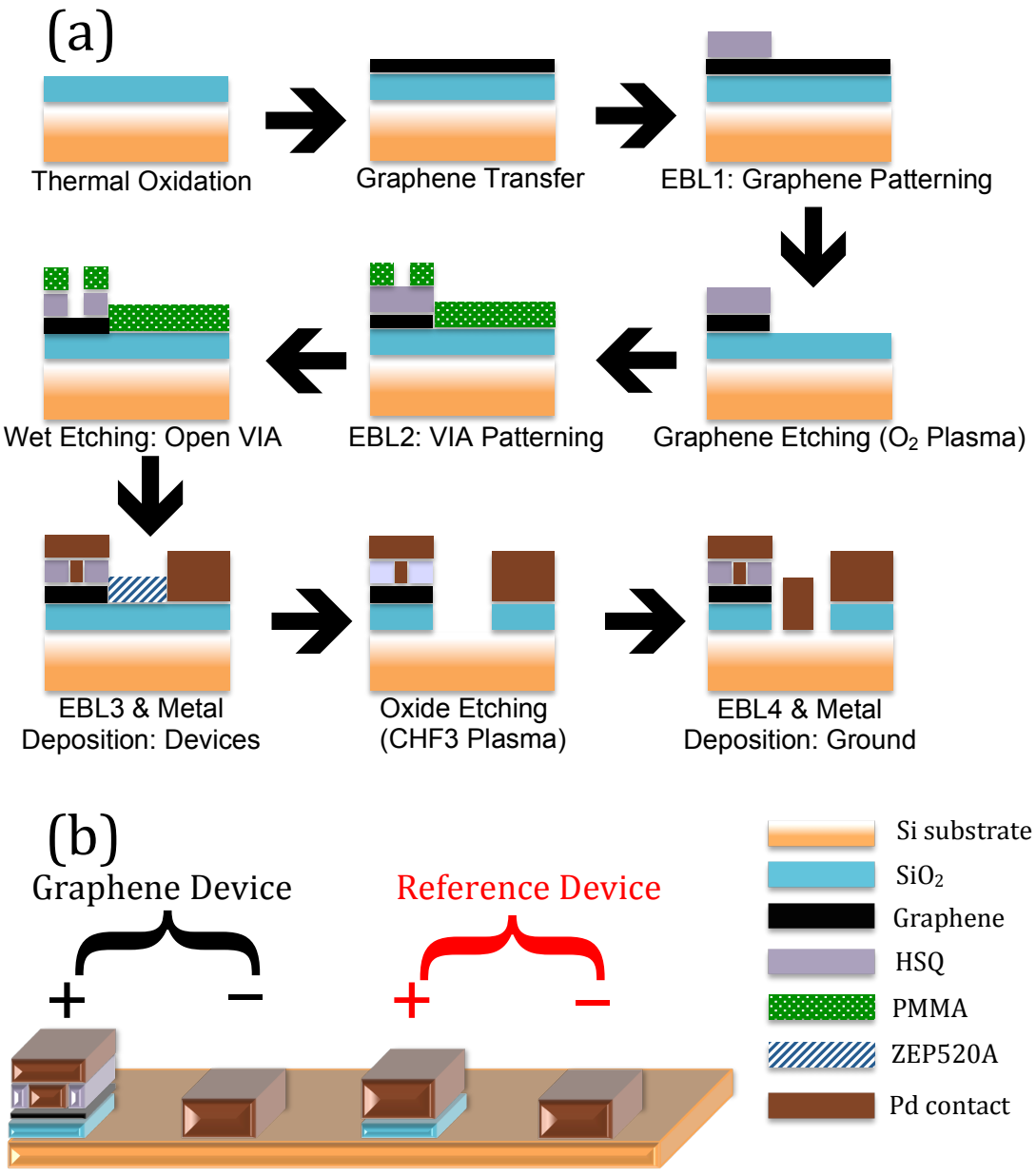


Figure 2-3: Illustration of the fabrication process flow of graphene-based floating gate memory devices

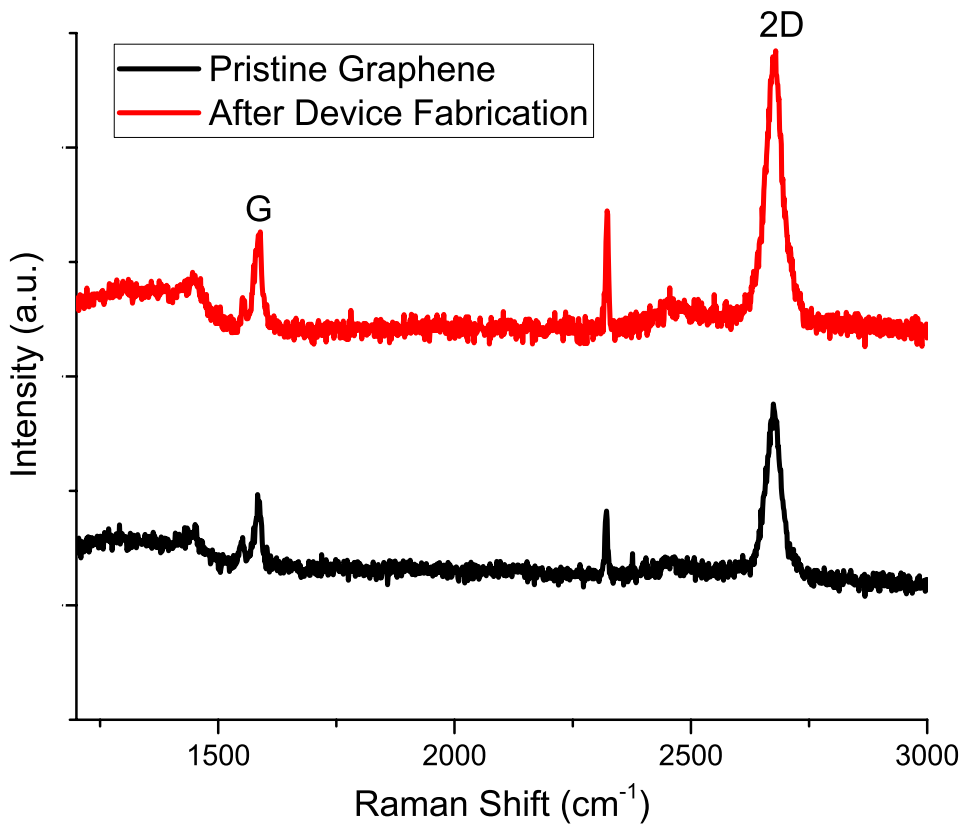


Figure 2-4: Raman spectra of CVD graphene sheets pristine and prior to metallization

2.3 Field Enhancement Factor Extraction

The average results from a set of 25 devices (both with and without graphene) are shown in Figure 2-5. Each of these devices was tested before and after electric current annealing. The current annealing was performed in accordance to the method given in [92]. The graphene devices exhibited a significantly lower turn-on voltage than reference devices, with curves for both devices shifted towards lower voltages after the current anneal. Namely, the turn-on voltage was reduced from ~10V to ~8V upon incorporation of graphene. Furthermore, the tunneling current for graphene-based devices was

significantly higher than the reference devices. This can be attributed to the electric field enhancement at the edges of graphene which concentrates the electric field due to accumulation of charges, as discussed in section 2.1, leading to an increase in the tunneling current [85, 87]. Furthermore, current annealing seems to further reduce the turn-on voltage of graphene-based devices to ~6V. This is partially due to removing the resist residues, H_2O vapor, and O_2 molecules that are introduced with each lithography step, which results in a more robust interface between the metal contact and the underlying layer and, in turn, improves the contact resistance. Current annealing also removes the resist residues from the grain boundaries of the CVD grown polycrystalline graphene layer leading to a better transport of charge carriers and a reduction in graphene's sheet resistance [92]. It is worth mentioning that the reduction in the turn-on voltage does *not* stem from the difference of the work function between graphene and Pd since this difference was measured to be only 0.1 eV [93] whereas the reduction in the turn-on voltage is 2V. This small difference in the work function was also asserted by Mueller *et al*. [94] who measured a potential step of only 0.1 eV at the graphene/Pd interface.

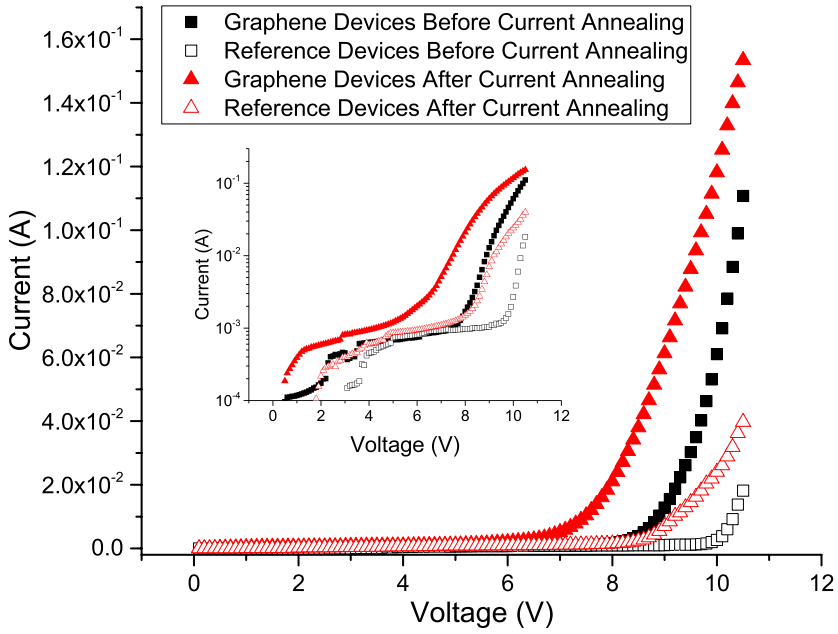
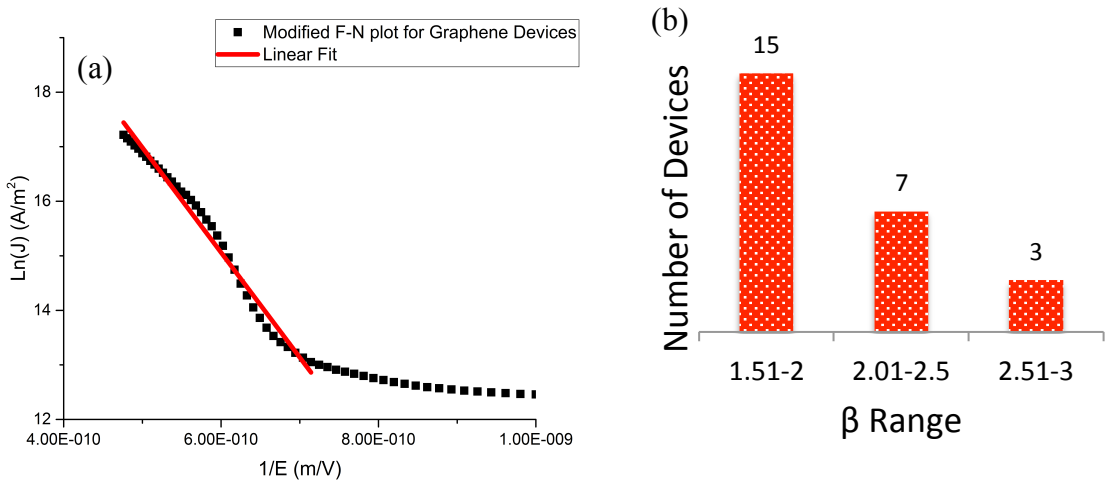


Figure 2-5: IV readings of floating-gate and reference devices before and after annealing

To extract the value of β using the modified FN equation (Equation 2-1), we need to plot ln(J) vs. (1/E), where $\ln(J) = \ln(a) - \frac{b}{\beta E}$. Our β is then read from the slope of the FN tunneling plot at a high electric field [43]. Figure 2-6a shows the FN tunneling plot for an average of 25 devices. The distribution of the value of β is shown in Figure 2-6b with a median value of 2.06 and a standard deviation of 0.33. This value agrees with the operating voltage of other graphene-based devices [16, 17]. We also extract β from the traditional FN model (Equation 1-2) to see whether the previously reported overestimated values of β were due to the model used. Towards this end, we plot $\ln(J/E^2)$ vs. (1/E), where $\ln\left(\frac{J}{E^2}\right) = \ln(a\,\beta^2) - \frac{b}{\beta E}$, and extract β in the same way as we did for the modified FN equation. In this case, the median value of β was found to be 2.85 with a standard deviation of 0.59. Figure 2-6c and Figure 2-6d show the FN tunneling plot and the

distribution of β, respectively, using the traditional FN equation. Although the value of β is slightly overestimated when using the traditional FN equation, the extracted values are much smaller than that previously reported. This suggests that the reason behind the overestimation of the previously reported values is not due to the model used. The overestimation of β in the other (non-device) reports might be due to depositing graphene on Si and Ti whose work functions are 1.5eV and 2eV lower than that of graphene, respectively. This in turn shifts the Fermi energy of graphene and lowers the barrier for tunneling [93]. In addition to that, previous reports used air as the tunneling dielectric, which is leakier than SiO_2 due to its low dielectric constant [47, 49-51].



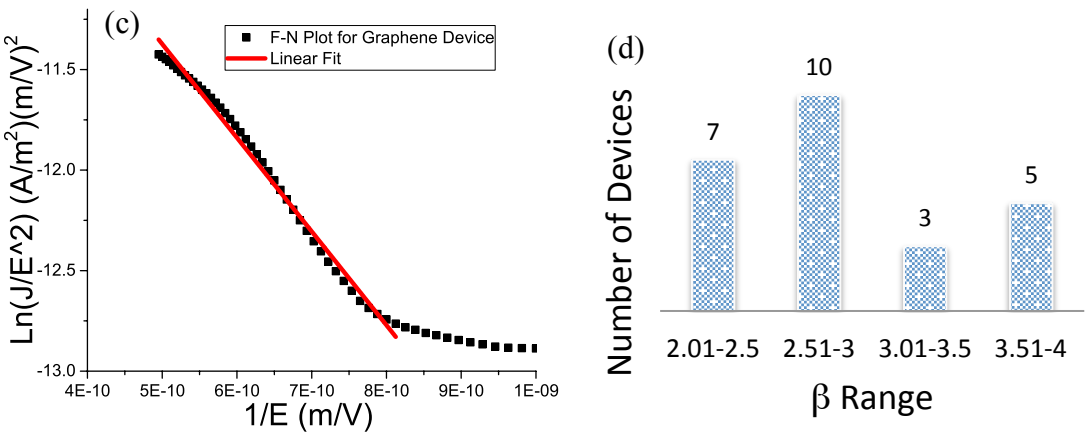


Figure 2-6: Field emission of a graphene capacitor device. (a) Modified FN tunneling plot, (b) Histogram showing the distribution of the field enhancement factor of multiple graphene devices based on modified FN tunneling equation, (c) Traditional FN tunneling plot, (d) Histogram showing the distribution of the field enhancement factor of multiple graphene devices based on traditional FN tunneling equation

2.4 Performance Analysis of Graphene NAND Flash

Regarding the implications of β for NAND flash, the capacitor device is tied to NAND flash operation through the control gate-coupling ratio (GCR). A graphene floating gate device model was created and HSPICE simulations were performed to identify the potential benefits of G-NAND. The G-NAND device is built by adding a capacitor atop of the gate of a CMOS transistor. Our transistor model is adopted from a predictive technology model (PTM) at the 65nm processing node [95]. The reason we use a relatively old technology node is to match the process during the fabrication. The capacitance value is properly set to be consistent with the oxide thickness assumed in PTM as well as the targeted thickness of tunneling dielectric of 10 nm and CG dielectric of 20 nm. Two voltage-controlled current sources are added between gate/source and

body/source, respectively, to mimic the tunneling current during the write and erase operations. Figure 2-7a shows a comparison of the ON/OFF resistance ratio for a 64-bit NAND string when the target cell is being read at the ON and OFF states. Our G-NAND is compared against a standard metal- or poly-based 2D NAND at the same 65nm process node. For a low write voltage of 6V, even for a long write pulse width of 1ms, the conventional floating gate devices cannot be written properly because of the low tunneling current. With a field enhancement factor of 3, the G-NAND string reaches the target ON/OFF ratio of 2 within 30μs thanks to the large effective field across the tunneling oxide, leading to a large tunneling current.

Under the same target ON/OFF ratio of 2, the write pulse and write voltage required are shown in Figure 2-7b for three different devices; conventional 2D NAND and G-NAND at β=2 and β=3. A trend of reduced write pulse width and write voltage is clearly seen as the value of β increases. A clear tradeoff exists between the write pulse width and the write voltage to reach the target ON-OFF ratio. By taking advantage of the large effective field of G-NAND, one can either (1) maintain the speed of the conventional floating gate devices with reduced write voltage as indicated by the red arrow or (2) keep a relatively large write voltage and significantly improve the write pulse width, hence a fast write operation, as indicated by the blue arrow.

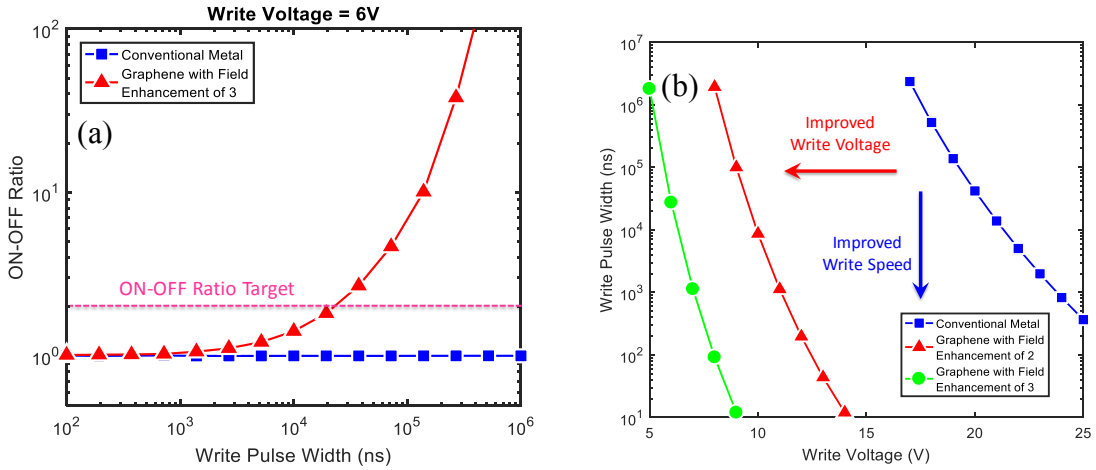


Figure 2-7: (a) The resistance ratio of the 64-bit NAND string at ON and OFF states versus the write pulse width at a given low write voltage of 6V, (b) The comparison of write speed vs. write voltage between the conventional metal and the graphene floating gate based flash with certain field enhancement factors for a given ON-OFF ratio of 2.

A reliability concern that emerges for G-NAND is the onset of pass disturbs. Due to the more efficient graphene FG layer, the pass voltage applied on nearby cells could induce a large tunneling current that may unintentionally write those pass transistors. To investigate the potential adverse effect of a large β, Figure 2-8 shows the maximum number of allowed read/write cycles before a potential failure, known as Program/Erase (P/E) cycles, for values of β = 2, 3, 4, and 5. Here, the potential failure is defined as the situation when the ratio of ON and OFF currents flowing through the nearby cells is less than 2 during their read operations. One can observe that the maximum number of cycles increases as the write voltage increases. This is because a large write voltage significantly reduces the write pulse width. Since the pass voltage remains the same, a short write pulse leads to fewer charges tunneling through the oxide of pass transistors. Therefore, for a given value of β, more P/E cycles can be achieved without a potential pass disturb.

For a P/E cycle target of 1000, one can benefit from a value up to $\beta = 3$ with a write voltage of >6V. If the field enhancement is too high, due to the large effective field across the tunneling oxide, the nearby cells will be unintentionally programmed within hundreds or even less number of read/write cycles.

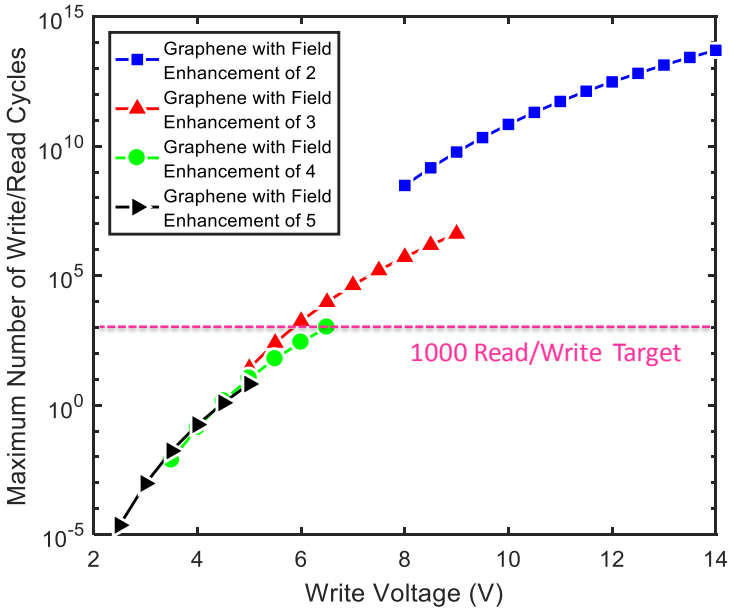


Figure 2-8: The maximum number of allowed read/write cycles before a potential failure due to the pass disturb versus the write voltage under various field enhancement assumptions of graphene-based flash devices.

2.5 Conclusion

The field emission from low-dimensionality materials can play a pivotal role in extending, or developing entirely new, NVM devices to meet the demands of advanced systems. In this work, 2D graphene sheets are experimentally benchmarked in a floating gate architecture and used to drive circuit-level simulation on a mature NVM technology,

64-bit 2D NAND strings. The field enhancement factor (β), at a barrier height of 3.1eV was shown to be 2.06 with a standard device-to-device deviation of 0.33. This modest value solves the contradiction in prior experiments that reported a field enhancement factor of few thousands but only 30-40% improvement in the write voltage of floating gate memory devices. We have used a modified Fowler-Nordheim (FN) model that is applicable to 2D materials to extract the field enhancement factor of graphene and compared the results to that obtained from the conventional FN model, where we found that the conventional FN model tends to slightly overestimate the value of β by about 30% compared to the modified FN model. This suggests that the overestimated β values reported previously are not caused by the extraction method and could be stemming from the fact that in earlier experiments graphene was deposited on metals whose work functions have a large mismatch (1.5-2 eV) with that of graphene, which in turn shifts the Fermi energy and lowers the barrier for tunneling. In addition to that, previous reports used air as the tunneling dielectric, which is leakier than SiO_2 due to its low dielectric constant. The role of this enhancement factor is to expand the operational design window for G-NAND and enable improved programming time and/or programming voltage down to 10ns and 5V, respectively, at a 65nm process node. NAND remains the dominant flavor of NVM and 2D materials, such as graphene, can expand the operational windows of floating gate and charge trap layers.

CHAPTER 3. HIGH MOBILITY SINGLE LAYER GRAPHENE

As mentioned in Chapter 1, Graphene is considered a promising novel interconnect material owing to its intrinsic electrical properties. Unfortunately, most of these properties are washed out by fabrication-induced damage, making real-life graphene devices a poor reflection of their theoretical benchmarks. In transitioning from traditional three-dimensional (3D) bulk materials to loosely adhered 2D graphene sheets, electrical properties can be lost in process steps that are commonplace to CMOS fabrication. It was observed that the possible roadblocks to graphene adoption within a commercial CMOS line are not all tied to the synthesis or even transfer process steps, but to fabrication damage post-transfer. Processing steps such as the stripping of multiple soft masks, spin/spray coating, and aqueous soaks induce tears, folds, and ultimately defects that cripple mobility and place device-to-device variability outside any acceptable commercial envelope.

Most recent fabrication advancements have focused on either the synthesis or transfer process steps of chemical vapor deposition (CVD) graphene [96]. CVD graphene is widely regarded as the most promising synthesis technique for large-scale integration. Specifically, pristine and uniform CVD graphene can be produced on Cu templates capable of supporting 200-300mm wafers [24]. Moreover, various transfer methods have been proposed to remove graphene sheets from their high-temperature synthesis template and apply them to a target wafer within the thermal budget of mainstream CMOS [97]. While both the quality of as-grown and as-transferred CVD graphene can be high, fabricated CVD graphene devices tend to exhibit relatively poor

mobility in the range of 2000-4000 $cm^2/V.s$ [14, 59-62]. These mobilities reflect only 10% of the theoretical phonon-limited mobility of graphene on SiO_2 (40,000 cm^2/Vs) [63].

In this chapter, we present a simple approach to fabricate high mobility CVD graphene devices [78]. The approach is based on using hydrogen silsesquioxane (HSQ) as a top dielectric to immediately pin down the CVD graphene sheet, post-transfer. This pinning dielectric provides a two-fold benefit: (1) mechanically anchors and protects the graphene and (2) provides a screening medium for charged impurities. In securing the graphene, peripheral issues related to the poor adhesion of contact metals to the graphene surface and mechanical abrasion at the graphene-SiO_2 interface during agitation are addressed. We then examine the feasibility of graphene interconnects for future IC technology nodes based on the ITRS roadmap. We specifically calculate the energy-delay product of graphene interconnects as a function of number of graphene layers with different edge roughness and benchmark them against copper interconnects. These calculations are performed by Dr. Chenyun Pan.

3.1 Fabrication Process of High-Mobility CVD Graphene

Figure 3-1 summarizes the fabrication process flow. The starting material is a 3cm × 3cm monolayer CVD graphene sheet atop 300nm of SiO_2 via a wet transfer process from ACS Materials. A 40nm film of 2% Hydrogen Silsesquioxane (HSQ) is spin-coated at 2000rpm for 60s with a ramp of 1000rpm/s. A JEOL JBX-9300FS Electron-Beam Lithography (EBL) System with a current of 2nA and a voltage of 100kV was used to pattern 10μm × 30μm rectangles. During exposure, the HSQ forms a thin

dielectric layer of dense, network-like, SiO_2 atop the graphene. The sample was then developed in MF-319 for 70s followed by 9:1 DI:MF-319 for 1min and then DI water for 1min. The sample is then dried with a light flow of N_2. Next, the HSQ pattern is transferred into the graphene layer using (Ar) plasma etch. Argon is used to avoid unintentional graphene doping from plasma species [98]. Whereas a normal process flow would strip the HSQ etch mask to apply metal contacts, we leave the HSQ as a dielectric to pin down the graphene and open vias to make metal contacts. A second EBL step, aligned to the HSQ, patterns both the vias and the metal pads. A 500nm film of ZEP520A resist was spin-coated at 2000rpm for 60s with a ramp of 1000rpm/s. The pattern was exposed with a dose of 500μC/cm^2, followed by development in Amyl Acetate for 120s and an IPA rinse with N_2 drying. Vias to the graphene surface are opened using the wet chemical etch described in Section 3.3. Finally, Ti/Au metal contacts (20/80nm) are deposited by Electron-Beam Evaporation followed by a standard liftoff procedure in 1165 at 120°C for 24hrs.

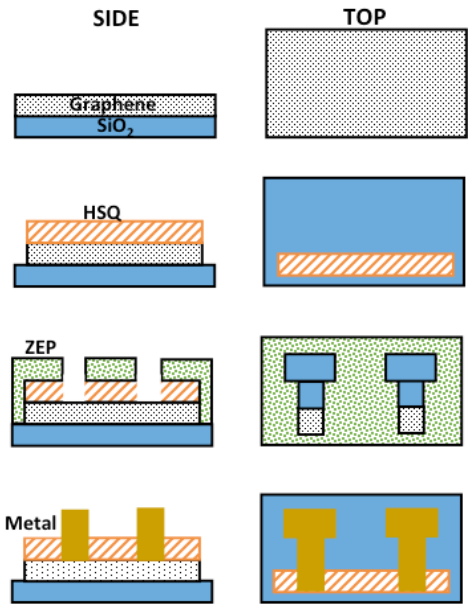


Figure 3-1: The general process flow for a dielectrically pinned CVD graphene. First, the starting material is CVD graphene on SiO_2. Next, EBL is used to pattern the graphene with HSQ. Next, the HSQ pattern is transferred into the graphene via a plasma etch. Next, a second EBL layer with ZEP is used to pattern vias and contact pads. Next, the vias are opened by clearing the HSQ using a wet etch. Next, contact metal is deposited using E-Beam. Finally, the excess metal is removed using a standard liftoff procedure.

3.2 Electrical Performance of Monolayer CVD Graphene

The transfer characteristics of a typical device are shown in Figure 3-2a. Electrical testing is performed under vacuum (1×10^{-3} Torr for 24hrs) in a Lakeshore probe station at room temperature. A Keithley 2612a source meter is used in a four-point configuration to remove any contact resistance from the readings. A pulsed back-gate technique is also used to remove potential hysteresis from charge trapping [99]. Mobility is extracted at a carrier concentration of 4×10^{12} cm^{-2} using the Drude model:

$$R_{ch} = \frac{L/W}{n\, q\, \mu}$$

$$n = \frac{C_{ox}\,(V_{BG} - V_{Dirac})}{q} \qquad (3\text{-}1),$$

where R_{ch} is the measured channel resistance, L and W are the length and width of the graphene ribbon, respectively, n is the carrier density, q is the elementary charge (1.602×10^{-19} C), μ is the carrier mobility, V_{BG} is the applied back-gate voltage, V_{Dirac} is the position of the minimum conductivity point, and C_{ox} is the oxide capacitance (11.6nF/cm^2 for the 300nm SiO_2 dielectric used in this work). Figure 3-2b illustrates the mobility distribution of the tested devices, showing an extracted mobility up to ~9,500 cm^2/V.s, which is twice the average value reported so far and among the highest recorded mobilities [59-62, 77]. Note that when using Drude model, the mobility should be extracted at a large carrier concentration to ensure its accurate determination [100]. It is worth mentioning that the yield of the fabricated devices was very low and only five devices were measured, out of which one device showed a mobility of 9,500 cm^2/V.s.

We also used the constant mobility model [100-102] to verify that the extracted mobility does not depend on the extraction technique and compare the experimental R-V_{BG} curve with that extracted from the constant mobility model (See Figure 3-2a). In the constant mobility model, the mobility is determined by fitting R_{tot} vs V_{BG} using equation (3-2) [102], where the constant mobility (μ_{const}) and charge impurity induced carrier concentration (n_0) are used as the fitting parameters. Note that the contact resistance (R_c) is set to zero in our case since it is already eliminated from four-probe measurements. We

found that the mobility values extracted using the Drude model at a carrier concentration of $4x10^{12}$ cm^{-2} agrees well with that extracted using the constant mobility model with an intrinsic carrier concentration of $2.5x10^{12}$ cm^{-2} which is in good agreement with the previously reported values ranging between $7x10^{11}$ and $3x10^{12}$ cm^{-2} [100]. Note that if we use the Drude model, the extracted mobility at a carrier concentration of $1.4x10^{11}$ cm^{-2} is ~25,000 cm^{-2}. However, using Drude model at such low carrier concentration is not accurate since the carrier concentration in this range is dominated by thermally-generated electron-hole pairs and electron-hole puddles [63, 83, 103] rather than back-voltage induced carriers.

$$R_{tot} = 2R_c + \frac{L/W}{\left(\sqrt{n_0^2 + n^2}\right).q.\mu_{const}} \quad (3\text{-}2),$$

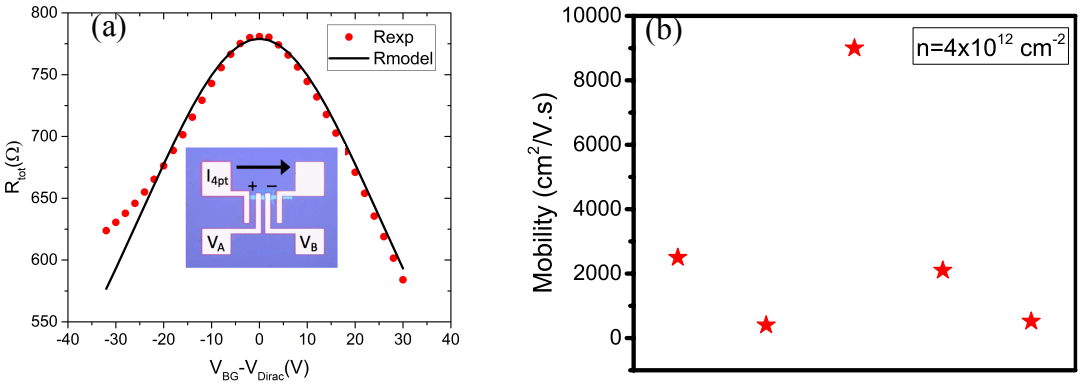


Figure 3-2: (a) Transfer characteristics from four-probe measurements on a typical pinned CVD graphene device. An optical image of the device is shown in the inset. Four-probe testing is performed by passing an excitation current around the outer pads and measuring the voltage drop across the inner pads, (b) Extracted carrier mobility for the tested devices at a carrier concentration of $4x10^{12}$ cm^{-2} showing a value up to 9,500 $cm^2/V.s$ which is twice the average value reported so far and among the highest recorded mobilities.

The high quality of these devices is attributed to the presence of the HSQ for two main reasons. First and foremost, HSQ acts as a screening layer for the charged impurities located in the SiO_2 substrate. The Fourier transform of the potential of a charged impurity is given by [104]:

$$V_i^0(q) = \frac{2\pi\, e^2}{\kappa\, q} \qquad (3\text{-}3),$$

where κ is proportional to the screening (dielectric) constant, which is the average dielectric constant of the material below and above the graphene sheet. In the absence of HSQ, the average dielectric constant is given by averaging the dielectric constant of SiO_2 (κ_{SiO_2}=3.9) and that of air (κ_{air}=1); that is κ_{avg}=(3.9+1)/2≈2.5. Adding HSQ (κ_{HSQ}=4) increases the average dielectric constant to ~4. From Equation (3-3), the potential created by the charged impurities is reduced and hence the force felt by an electron flowing across the graphene interconnect is reduced, which in turn minimizes scattering. Earlier reports have shown that high-k mediums atop graphene lead to a sharp R-V_{BG} curve; hence improving mobility [105]. Furthermore, the screening of charged impurities also eliminates the asymmetry between electron and hole mobilities since this asymmetry was shown to originate from the different scattering cross sections for electrons and holes by the charged impurities [106].

Secondly, HSQ acts as a pinning dielectric. This overlying dielectric mechanically anchors and protects the graphene sheet from process damage. Moreover, the relatively weak adhesion between graphene and SiO_2 (~0.2 J/m^2) [107] opens avenues

for shifting and abrasion at the graphene-SiO_2 interface during mechanically aggressive process steps [107]; specifically, spin/spray coating, aqueous soaks, and depositions. Pinning down graphene to the substrate allows for an accurate patterning of structures. It also improves the back-gate control of graphene and enhances its contact resistance. Figure 3-3 compares a device array that followed a non-pinned process flow (same synthesis and transfer process) with a device array fabricated using HSQ pinning. For the unpinned devices, metal contacts (Ti/Au) are patterned directly onto the CVD graphene sheet using EBL with ZEP520A. Despite good adhesion between the Ti and graphene surface, the metal pattern provides and optical indicator of the degree of graphene sheering from the SiO_2 surface. It is worth mentioning that HSQ specifically provides a very appealing material to be used as a top layer on graphene for the following reasons: (1) it saves extra fabrication steps by being an e-beam pattern for the graphene devices as well as providing dielectric screening and mechanical anchoring, (2) it is deposited on graphene by spin-coating which introduces the least number of defects to graphene compared to other methods such as e-beam evaporation and RF sputtering [108], and (3) due to the high tunability of its dielectric constant based on the degree of cross-linking [109].

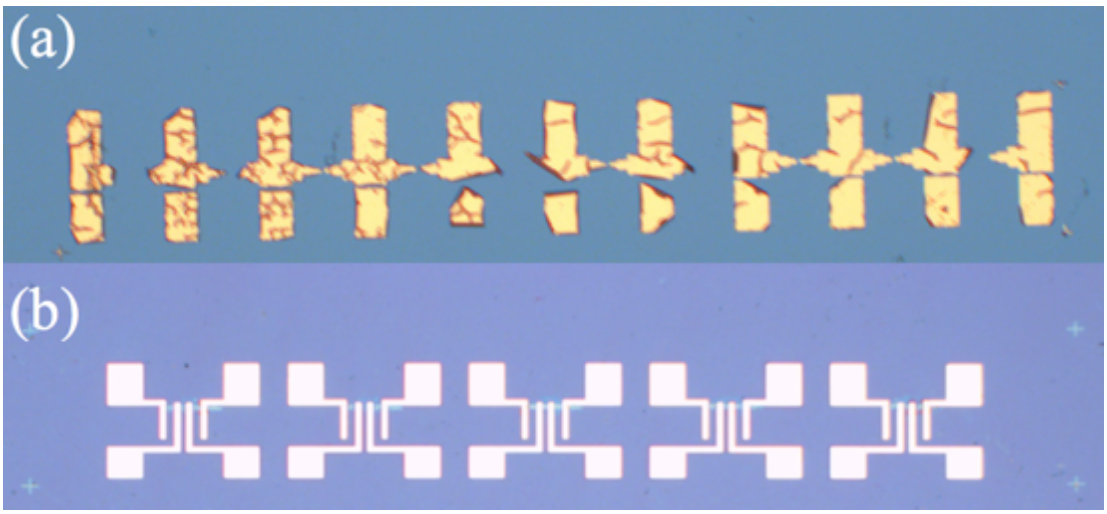


Figure 3-3: (a) Optical image of an array of CVD graphene devices fabricated without a pinning dielectric. Following the metallization liftoff, rips, tears, and folds are visible in the devices, (b) Devices fabricated after HSQ pinning. Note the absence of tears and folds in the latter case.

Figure 3-4 compares the Raman spectra of graphene devices after fabrication with that of pristine graphene. Upon fabrication of graphene devices, the D to G peak intensity ratio (I_D/I_G), which signifies the degree of disorder in graphene, increased from 0.08 to 0.56. Despite the increase in I_D/I_G ratio, the defect density in the fabricated graphene devices is still considered low [110, 111]. The point defect density in graphene can be quantified as [112]:

$$n_D(cm^{-2}) = \frac{(1.8 \pm 0.5)\times 10^{22}}{\lambda_L^4}\left(\frac{I_D}{I_G}\right) \qquad (3\text{-}4),$$

where λ_L is the excitation laser wavelength (in nanometers). From Equation (3-4) and using an excitation wavelength of 488 nm, n_D for pristine and fabricated graphene are 2.65×10^{10} cm^{-2} and 1.76×10^{11} cm^{-2}, respectively.

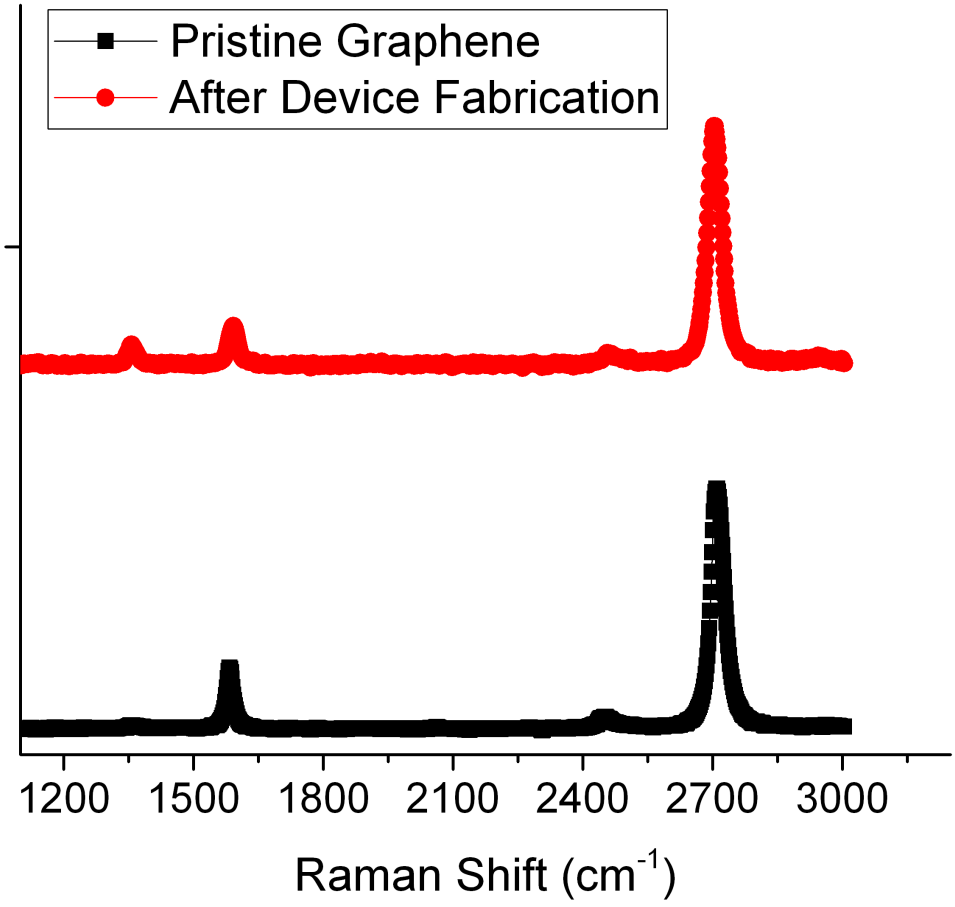


Figure 3-4: Raman spectra of graphene before and after fabrication. Note that the defect density increases after fabrication due to the compressive stress that HSQ exerts on graphene which can, in turn, create vacancies, dislocations, and/or dangling bonds. The presence of compressive stress is confirmed from the blue shift of the G-peak after device fabrication from 1583.2 cm^{-1} to 1592.8 cm^{-1}.

The increase in the defect density is partially attributed to the compressive stress that HSQ exerts on graphene which can, in turn, create vacancies, dislocations, and/or dangling bonds. The presence of compressive stress is confirmed from the blue shift of

the G-peak after device fabrication as shown in Figure 3-4 where the G-peak is blue-shifted from 1583.2 cm^{-1} to 1592.8 cm^{-1}. Using a biaxial stress model, the G band stress coefficient is estimated to be 7.47 cm^{-1}/GPa [113]. Thus, the compressive stress on the fabricated graphene devices is calculated to be 1.29 GPa. This is the main reason why our reported mobility is still falling behind the theoretical limit of 40,000 cm^2/V.s. We believe that optimizing the e-beam dose during lithography would decrease the compressive stress on graphene since the dose determines the degree of HSQ cross-linking. However, a more detailed study is still needed.

3.3 Controlling the Etch Rate of HSQ

HSQ must be effectively cleared to insure robust contacts are made to the graphene surface. We studied the etching of HSQ using different etchants, including fluoride-based etchants due to the similarity in the chemical structure between HSQ and SiO_2. Various concentrations of hydrofluoric acid (HF) were used: 199:1 H_2O:HF made from 199 parts H_2O and one part 49% HF, 149:1 H_2O:HF made from 149 parts H_2O and one part 49% HF, 24:1 H_2O:HF made from 24 parts H_2O and one part 49% HF, 9:1 H_2O:HF made from 9 parts H_2O and one part 49% HF, 5:1 H_2O:HF made from 5 parts H_2O and one part 49% HF, and 6:1 Buffered Oxide Etch (BOE) made from 6 parts 40% NH_4F and one part HF. We also studied the size-dependency by patterning rectangles of sizes 200μm×20μm, 400μm×40μm, and 800μm×80μm. To study the variability of the etching rate among the structure, we measured 20 samples from each size of the tested structures. HSQ was spin-coated on a degenerately p-doped Si substrate with a 300nm of thermally grown SiO_2 layer. Prior to the spin coating of HSQ, a thin Cr layer (100nm) is evaporated on SiO_2 which acts as a barrier layer and prevents the etchant from reaching

the SiO_2 substrate, hence allowing for the accurate determination of the HSQ etch rate since SiO_2 is sensitive to fluoride-based etchants.

F^- based etchants effectively removed HSQ with an etching rate exceeding 40 nm/s for most of the concentrations studied. A low F^- ion concentration (less than 149:1 H_2O:HF) should be used if an accurate control of the etching process is required. Table 3-1 summarizes the etching rate of different etchants for 800μm×80μm structures. It should be noted that the etch rate did not show a significant dependence on the pattern size with the etching rate being within 3% for all the studied sizes. 199:1 H_2O:HF has the lowest etching rate of 10.3 nm/s with a standard deviation of 1.3 nm/s; hence, this concentration should be used if an accurate control of the etching process is required. Higher F^- concentrations can be used if the etching process is not critical and a fast etching is needed. Table 3-1 also emphasizes the non-linear increase of the etching rate as a function of F^- ion concentration. Also, the etching rate stayed constant at the beginning of the etching process then it drops down (Figure 3-5). This is probably because the fresh surface of HSQ allows F^- ions to attack the Si ions in HSQ hence causing etching. Afterwards, a SiF layer is created on the surface of HSQ, which slows down the etching process.

Table 3-1: Etching rate of 800μm×80μm HSQ structures for different F^- based etchants

Etchant	Etching Rate (nm/s)	Standard Deviation (nm/s)
199:1 H_2O:HF	10.3	1.3
149:1 H_2O:HF	21.5	1.8
24:1 H_2O:HF	>40	-
6:1 BOE	>40	-

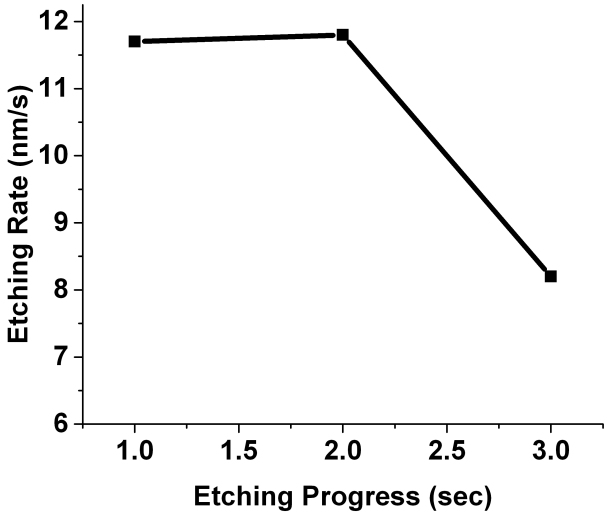


Figure 3-5: Progress of etching rate for 800μm×80μm HSQ structures. The etching rate stayed constant at the beginning of the etching process then it drops down probably because the fresh surface of HSQ allows F^- ions to attack the Si ions in HSQ hence causing etching. Afterwards, a SiF layer is created on the surface of HSQ, which slows down the etching process.

3.4 Interconnect Performance Projections of CVD Graphene

To obtain the current in a graphene interconnect, Landauer formula can be used as [114]:

$$I = \frac{q}{h}\int_{-\infty}^{\infty} 2 \sum_{m} \frac{l_{eff}}{L + l_{eff}} [f(E - \mu_1) - f(E - \mu_2)\, dE] \quad (3\text{-}5),$$

where h is Planck's constant, q is the elementary charge, L is the length of the interconnect, f is the Fermi distribution function, μ_1 and μ_2 are the electrical potential on each side of the graphene, E is the energy level, m is the number of subbands, assuming a semiconducting armchair graphene [18], and l_{eff} is the effective mean-free-path (MFP) of the graphene, which is extracted based on the analytical equation that is written as [115]:

$$MFP = \frac{\hbar}{q}\, \mu \sqrt{n\, \pi} \quad (3\text{-}6),$$

where $\hbar$ is the reduced Planck's constant, μ is the mobility extracted from the experiment, n is the carrier concentration that is calculated by $n = \frac{\epsilon_0\, \epsilon_r}{t_{ox}}\, V_{BG}$, and V_{BG} is the applied back-gate voltage. The corresponding Fermi energy of the graphene, E_F, can be obtained based on the model, shown as [116]:

$$E_f = \frac{1}{\gamma\, t_{ox}} \left(\sqrt{\epsilon^2 + 2\, \gamma\, \epsilon\, q\, V_{BG}\, t_{ox}} - \epsilon\right) \quad (3\text{-}7),$$

where $\gamma=(4\pi q^2)/(h^2 v_F^2)$ is a constant depending on graphene properties, and $v_F \approx 10^6 \mathrm{m/s}$ is the Fermi velocity.

Based on Equations (3-5) - (3-7), the resistance calculated based on quantum transport theory matches well with the experimentally measured data, shown in Figure 3-6a, and Figure 3-6b show the extracted MFP at various carrier concentrations. This demonstrates the consistency of the simulation approaches used.

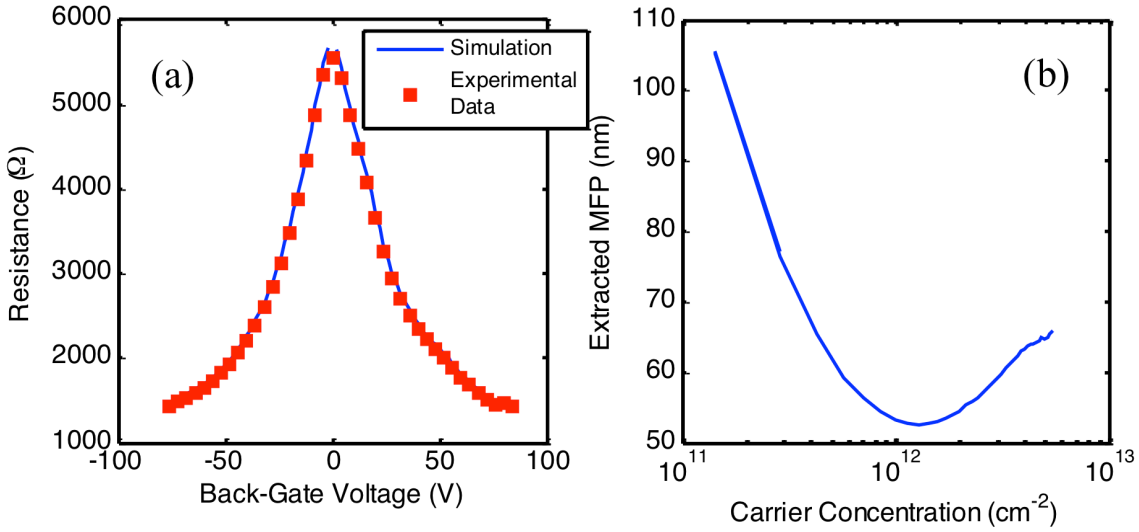


Figure 3-6: (a) Comparison between experimental measured resistance and simulation results based on extracted MFP values from the experiments for various back-gate voltages. (b) Extracted MFP versus carrier concentration.

Since the resistance per unit length of a single-layer graphene is much larger than that of a copper wire, multi-layer graphene interconnects are considered in this work. The Fermi energy is chosen as 0.35eV. Previous work has shown both theoretically and experimentally that top contacts cannot fully utilize the potential benefits of multilayer graphene interconnects because the current needs to be redistributed to other graphene

layers through the interlayer resistance, which reduces the overall conductivity [64, 73]. Therefore, in this work, side contacts that electrically connect to all graphene layers are assumed to be possible. As the interconnect dimension scales down, the resistance per unit length of copper increases dramatically because of 1) the smaller cross-sectional area, 2) the severe size effects, and 3) the thick diffusion barrier that takes an ever-increasing fraction of the wire volume [117]. Therefore, we investigate the potential benefits of graphene interconnects at the sub-10nm dimensions at the end of ITRS [118]. The MFP of graphene is based on the experimentally extracted value in this work, assuming smooth edges. The capacitance value is estimated based on the quantum capacitance and the electrostatic capacitance, which are adopted from the previous work [119]. The contact resistance is 100 Ω·μm based on the previous experimental values [120].

The intrinsic interconnect energy-delay product versus the number of graphene layers is shown in Figure 3-7. The interconnect width and length are 7nm and 5μm, respectively. Three different MFPs relative to the experimentally extracted value are explored and compared. In addition, two different edge smoothness are investigated, including perfect edge and edge scattering probability of 0.2, which is measured in the experiment [121].

Optimal numbers of graphene layers exist to achieve the minimum intrinsic interconnect energy-delay product (EDP). This is because when the number of graphene layers is small, the large resistance of the graphene interconnect dominates the delay and increasing the number of graphene layers significantly reduces the interconnect resistance. However, if there are too many graphene layers, the line-to-line capacitance

increases significantly, overshadowing the benefits of the resistance saving. Therefore, the improvement starts to decrease when the number of layers is beyond a certain point. To achieve a comparable intrinsic delay with copper interconnects, the edge smoothness is crucial based on the comparison between Figure 3-7a and Figure 3-7b.

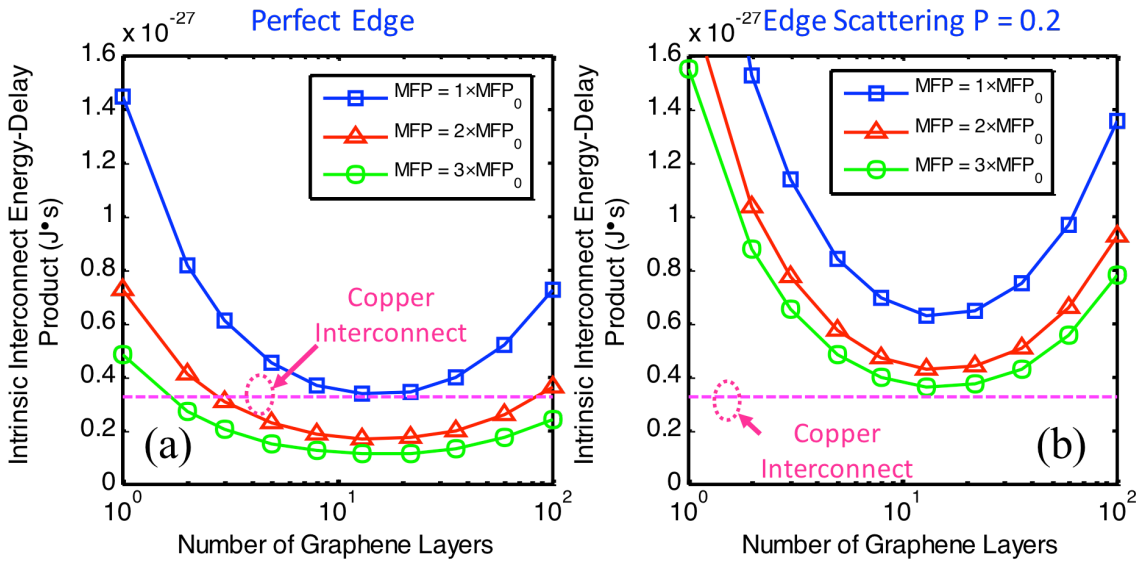


Figure 3-7: Intrinsic interconnect energy-delay product versus the number of graphene layers for various MFPs with (a) perfect edge and (b) edge scattering probability of 0.2.

To explore the potential benefits of various hypothetical MFPs relative to the experimentally extracted data, the percentage of the improvement in EDP compared to copper are investigated for three different wire widths, shown in Figure 3-8. The improvement increases at a narrow dimension as a result of the significant increase of the copper interconnect resistivity due to the size effects. If the MFP can be further improved, up to 80% of the EDP can be saved for a smooth graphene interconnect with 3× of the experimentally extracted MFP value at the width of 5nm. From Figure 3-8b, the

edge roughness of the graphene significantly reduces its advantage over the copper interconnect, where at least 2× of the experimentally extracted MFP value is required for a 5nm wide graphene interconnect to achieve a better EDP.

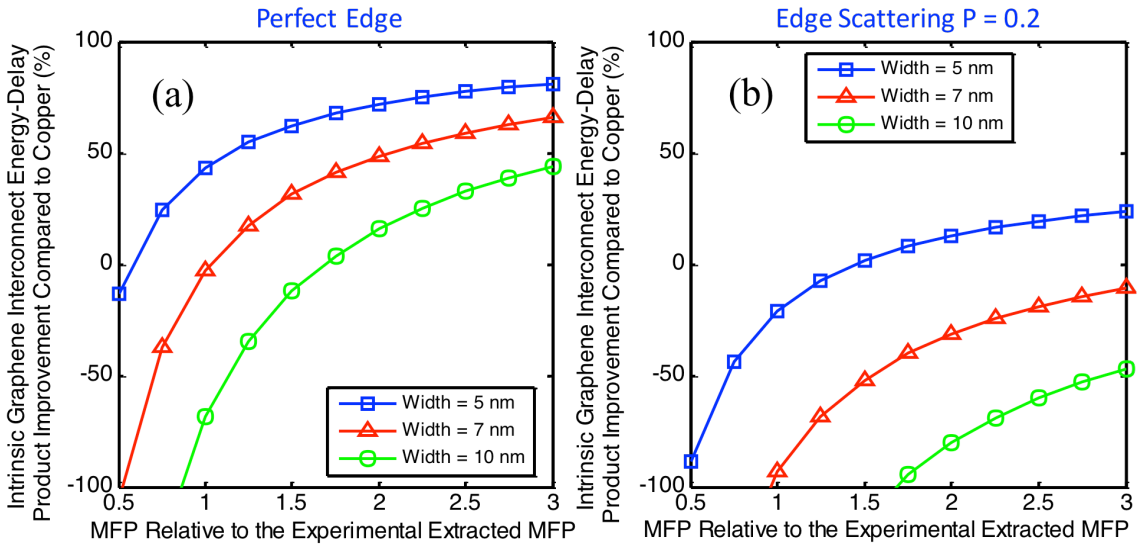


Figure 3-8: Intrinsic interconnect energy-delay product improvement versus the MFP of graphene for three different interconnect widths with (a) perfect edge and (b) edge scattering probability of 0.2.

3.5 Conclusion

In summary, a simple two-step lithography process to fabricate graphene devices with mobilities up to ~9,500 $cm^2/V.s$ at a carrier concentration of $4x10^{12}$ cm^{-2} has been presented. The high quality of these devices is attributed to the presence of an HSQ pinning dielectric that is applied immediately after the transfer step. This dielectric anchors the loosely bound graphene sheet to the SiO_2 surfaces, primarily screening local charged impurities and secondarily reducing process damage. Peripheral process development with the spin-on glass, HSQ, was presented. F^- based etchants were shown

to be very effective HSQ etchants with an etching rate that can exceed 40nm/s. A low F^- ion concentration (less than 149:1 H_2O:HF) should be used if an accurate control of the etching process is required. The proposed fabrication method is expected to bring new focus to post-transfer passivation of CVD graphene as a means of improving quality and suppressing device-to-device variation. The potential benefits of graphene interconnects are evaluated based on the MFP extracted from the experimental data. Even though the reported mobility is more than 2x higher than the average recorded mobility, MFP analysis shows that the MFP attained still needs to at least be doubled in order to achieve a significant improvement in the energy-delay product compared to copper interconnects. This means that we should further improve the mobility to reach around 20,000 $cm^2/V.s$. Possible methods to achieve such a high mobility are to optimize the dielectric constant of HSQ and/or replace the SiO_2 underneath graphene with a high-k dielectric. Also, better performance can be achieved by considering multilayer graphene instead of single layer graphene.

CHAPTER 4. ACCURATE DETERMINATION OF INTERLAYER RESISTIVITY IN MULTILAYER CVD GRAPHENE

As mentioned in the previous chapter, in order to achieve a significant improvement in the energy-delay product compared to copper interconnects, the electron mobility of monolayer CVD graphene on SiO_2 should be around 40,000 $cm^2/V.s$. Knowing that the theoretical limit of the mobility of monolayer CVD graphene on SiO_2 is also 40,000 $cm^2/V.s$ [63], it is almost impossible for monolayer CVD graphene interconnects to provide a substantial reduction in the energy-delay product compared to their Cu counterpart due to fabrication-related imperfections.

Using multilayer graphene (MLG) interconnects can potentially provide a lower resistance and probably lower energy-delay product compared to single layer graphene (SLG) interconnects. This is because MLG provides more conduction paths compared to SLG [64]. However, MLG has larger capacitance and therefore the number of graphene layers should be optimized to minimize the RC delay. Figure 4-1a**,** which is taken from [64], illustrates the RC delay of MLG as a function of number of layers. Initially, the delay decreases by adding more layers due to decreasing the effective resistance. An optimum point is reached beyond which the delay increases due to an increase in the capacitance. Also, the energy dissipation increases by increasing the number of layers since it is directly proportional to the capacitance according to the equation:

$$E = \frac{1}{2}(C_S + C_L + c_w L)V_{DD}^2 \quad (4\text{-}1),$$

where C_s is the source parasitic capacitance, C_L is the load capacitance, c_w is the capacitance per unit length, L is the interconnect length, and V_{DD} is the supply voltage. Therefore, the energy-delay product initially decreases by increasing the number of layers reaching a minimum value then increases again due to increasing energy dissipation as shown in Figure 4-1b [64].

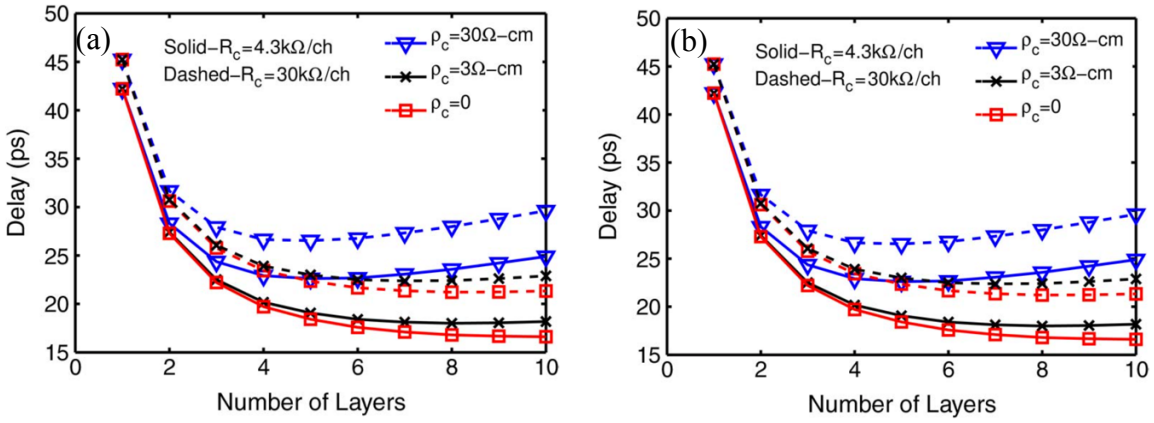


Figure 4-1: (a) Delay and (b) Energy-Delay Product versus number of graphene layers for various values of interlayer resistivity, ρ_c. The analysis is also done for two different values of contact resistance-4.3 kΩ per channel and 30 kΩ per channel [64].

The overall resistivity of MLG is determined by two parameters: an intralayer resistivity (ρ_a), which represents the resistance of each graphene layer along the length of the sheet, and an interlayer resistivity (ρ_c), which arises from the coupling between the individual graphene layers. For top-contacted MLG interconnects, the interlayer resistivity is one of the important intrinsic parameters affecting the performance of MLG interconnects. This is because for a relatively small interlayer resistivity, electric current

tends to redistribute itself among the different layers more easily. For instance, Figure 4-2 [65] shows how current is distributed in a bi-layer graphene interconnects with a top contact if the in-layer resistances of the two layers are the same. It can be seen that for ρ_c=3 Ω-cm, the current is split equally between the two graphene layers after 0.8 μm away from the contacts whereas it takes 2 μm for that to happen if ρ_c=30 Ω-cm. This suggests that MLG would be suitable for short interconnects (local interconnects) only if ρ_c is small. Otherwise it would be more desirable to use MLG only for long interconnects. Additionally, ρ_c affects the delay and energy-delay product as shown in Figure 4-1. For the same number of layers, the delay increases with increasing ρ_c because the effective number of conduction channels is reduced. It is worth mentioning that for side-contacted MLG, the interlayer resistivity has a minimal effect on the performance since side contacts can directly connect to all layers simultaneously, leading to a distribution of current in various layers according to the resistance of each layer. However, the fabrication process of side-contacted graphene is more involved [122, 123].

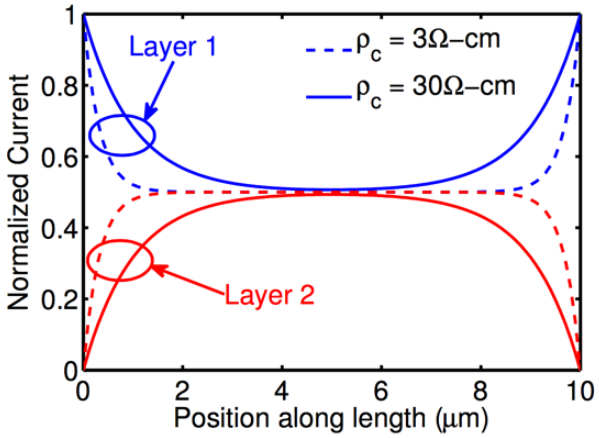


Figure 4-2: Normalized Current Distribution between two layers along the length of the interconnect, shown for two different values of ρ_c.

4.1 The Riddle of Interlayer Resistivity

It is clear that the value of interlayer resistivity (ρ_c) greatly affects the performance of MLG interconnects. For this reason, it is important to understand its origin and accurately determine the value of ρ_c so that MLG interconnects can be optimized accordingly. Several theoretical and experimental studies have been conducted to determine the value of the interlayer resistivity and compare it with the in-layer resistivity. Wallace used tight binding method to study the interaction between adjacent layers in graphite [66]. He found that the interlayer resistivity depends on the exchange potential between the electrons in the adjacent layers. This, in turn, suggests that the interlayer resistivity depends on the overlap between the p_z orbitals in the adjacent layers. Therefore, interlayer resistivity should be greatly affected by stacking faults between adjacent layers since a large misorientation angle between adjacent layers would lead to a smaller overlap between the p_z orbitals and lead to a relatively large ρ_c. This mechanism was also suggested by Uher and Sander [69] and Habib *et al.* [70] who also attributed large ρ_c values to the stacking faults between graphite layers. In fact, Habib *et al.* [70] showed that ρ_c monotonically increases by increasing the misorientation angle between adjacent layers in bilayer graphene. Other studies suggest that the large value of ρ_c stems from localized states along the c-axis of graphite [67]. A more recent study shows that ρ_c is affected by lattice defects that enhance the electronic coupling between the layers giving rise to a quasi-3D electronic spectrum with coherent transport along the c-axis [68]. Furthermore, it was shown that ρ_c is a function of the Fermi energy [70], which, in turn, is a function of doping.

Unfortunately, the reported values for interlayer resistivity vary by several orders of magnitude [67, 69, 73], which hampers the accurate modeling of the performance of MLG interconnects and can lead to misleading analyses. For example, Morgan and Uher [67] measured ρ_c to be as small as 1×10^{-3} Ω.m whereas Sui and Appenzeler [73] reported a value of 0.3 Ω.m, which is two orders of magnitude larger. Furthermore, Uher and Sander [69] showed that ρ_c changed by one order of magnitude between the different samples that they measured. The disagreement between the different reported values can be partially attributed to the quality of the samples and possibly due to difference in the extent of stacking faults of adjacent graphene layers [67, 69, 71]. Also, some of the measured graphite crystals were not exactly rectangular in the xy plane, so the dimensions used to calculate ρ_c were not exact [72]. However, one important factor affecting this disagreement is the method by which the interlayer resistivity is measured. All the aforementioned experiments used four-probe measurement technique to extract the resistance where they put two contacts on each side of a thick graphite sample and apply a vertical electric field across it, as illustrated in Figure 4-3a. This vertical electric field was shown to modify the band structure of graphite [74] which can potentially alter the effective mass of electrons in the c-direction and, in turn, affect the value of ρ_c. Furthermore, measurements should be done on graphene samples rather than graphite because their band structures and their effective masses are different, which would lead to different ρ_c values. This suggests that more accurate measurements of ρ_c need to be done in order to accurately analyze MLG interconnects. It is worth mentioning that Kim *et al.* [75], measured the interlayer resistivity of twisted bilayer graphene (BLG) by fabricating a graphene cross junction where two exfoliated monolayer graphene strips are transferred

on top of each other and the resistance is measured at the overlap region. They extracted an interlayer resistivity of ~2000 Ω.cm at 280K. Although their study provided a very good insight on the range of interlayer resistivity in exfoliated BLG, it did not provide a full picture of the variation of interlayer resistivity as a function of twist angle as well as the number of graphene layers.

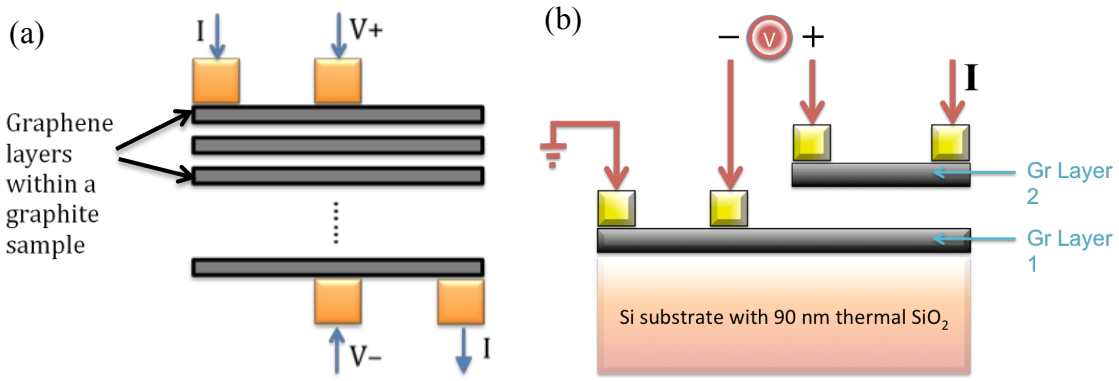


Figure 4-3: Schematic diagram of (a) conventional method to measure interlayer resistivity of graphene, (b) our proposed method. Note that in (b) the current is injected from the bi-layer and collected at the monolayer region, ensuring the flow of current through both layers.

4.2 Proposed Structure to Measure the Interlayer Resistivity in Graphene

We propose an accurate method of measuring the interlayer resistivity of top-contacted MLG. We systematically study how interlayer resistivity evolves with increasing the number of graphene layers (up to four layers) as well as the twist angle between them. Four-probe technique is implemented on a graphene ribbon, which has more number of layers on one side compared to the other side as shown in Figure 4-3b. Current is injected from the side that has more graphene layers to that with fewer layers.

This ensures that the charge carriers cross between the layers allowing for the measurement of interlayer resistivity. The voltage is measured across the interface between the two graphene regions. The measured data is fed to a distributed resistance model where the interlayer resistivity is extracted. The extracted interlayer resistivity is used to assess the electrical performance of multilayer graphene interconnects in terms of delay, energy dissipation, and energy-delay product. Dr Chenyun Pan developed the distributed resistance model as well as provided the simulated electrical performance of graphene interconnects. This method is generic and can be applied to any two-dimensional layered materials such as metal dichalcogenides.

4.3 Fabrication Process and Device Characterization of CVD Multilayer Graphene

4.3.1 Graphene Growth and Transfer

Graphene was grown on Pt foil in a vertical cold-wall AIXTRON Black Magic Pro 6″ CVD system. Graphene was transferred to SiO_2 substrate with wet transfer process. Pt/graphene sample was submerged in 80°C UPW for 16h to achieve water intercalation. A support polymer (e.g., PMMA) was first spin-coated on the Pt/graphene. Then Graphene/PMMA was delaminated from Pt foil by electrolysis in NaOH (0.2 M) at −3V. The sample was rinsed in UPW and subsequently annealed in vacuum at 50°C overnight. Finally, the PMMA supporting layer was dissolved in hot acetone at 50°C overnight. More details about graphene growth and transfer are published somewhere else by Verguts *et al.*[124].

4.3.2 Device Fabrication

Graphene was patterned into rectangular structures using Electron Beam Lithography (EBL) where a film of 2% Hydrogen Silsesquioxane (HSQ) is spin-coated at 4000rpm for 60s with a 3s ramp on top of a PMMA 3C film spin-coated at 4500rpm for 60s with a 3s ramp. After EBL exposure, the sample is developed in OPD5262 for 60s followed by DI water rinse and N_2 blow drying. The sample is then subjected to a 100W O_2 plasma for 8 minutes to etch the graphene that is not protected by the HSQ, creating 16μm × 7μm rectangular structures. The PMMA layer acts as a sacrificial layer to protect the underlying graphene from the damage that would occur if the HSQ layer were to be removed by plasma etching. The PMMA/HSQ resist stack can be removed by leaving the sample in hot acetone (at 50°C) for two hours followed by IPA rinse. A 30nm of PECVD-grown SiO_2 is then deposited on top of graphene and then a second EBL step is done to open 16μm × 3μm rectangular structures in SiO_2 to ensure purely top contacts. PMMA resist is used to pattern these structures and protect the SiO_2 areas outside these rectangles from being etched. The exposed SiO_2 regions are etched in a 1%HF solution for 15 seconds then rinsed in a DI-water bath. A third EBL step is employed to create the metal contacts where the sample is first prebaked at 120 °C on a hotplate for 5 minutes. After that, a PMMA in 3% chlorobenzene resist is applied to the sample by spin coating at 4500rpm for 45s. After EBL exposure, the sample is developed in 1:1 MIBK:IPA for 50s followed by a 30s IPA dipping. 50nm thick Pd contacts are deposited using e-beam evaporation followed by an overnight liftoff process in hot acetone. Figure 4-4 illustrates a schematic of the fabricated top-contacted graphene ribbons.

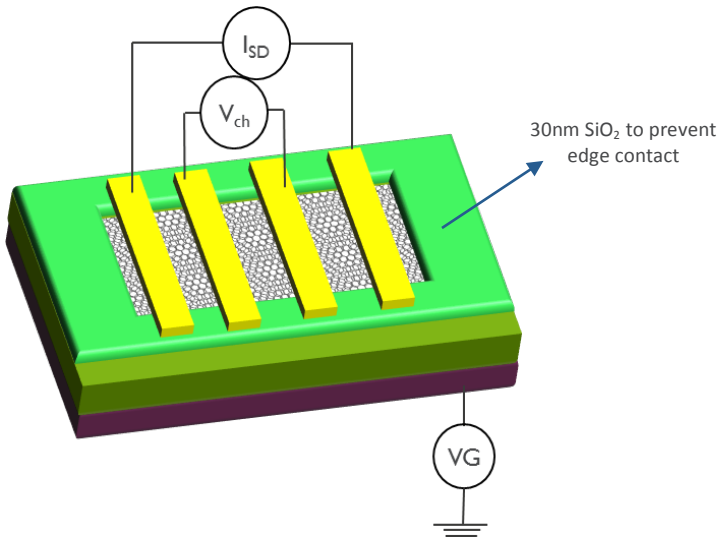


Figure 4-4: Schematic diagram illustrating top-contacted graphene.

4.3.3 Device Characterization

The number of graphene layers was determined using a combination of optical microscopy and Raman spectroscopy. A 532nm laser was used for the Raman measurements. Four probe measurements were carried out in a back-gate configuration under an N_2 rich ambient.

4.4 Experimental Analysis of Fabricated Multilayer CVD Graphene Devices

Figure 4-5a shows an SEM image of a typical device and Figure 4-5b shows the Raman spectra for different bilayer graphene devices with different twist angles. In order to ensure a purely top contact, the graphene edges are covered with a 30nm of PE-CVD-grown SiO_2 layer as shown in Figure 4-4 as well as Region I of Figure 4-5a. Region II in Figure 4-5a represents the exposed graphene area on which Pd contacts are deposited. As shown in Figure 4-5b, SLG is designated with a sharp 2D peak (FWHM=36cm^{-1}) and 2D/G ratio that is greater than 1. On the other hand, AB-stacked BLG has a broader 2D

peak with a FWHM of 54.2cm^{-1} and 2D/G ratio less than 1, which is typical for multilayer graphene [108]. As the twist angle between the graphene layers increases, the FWHM of the 2D peak decreases until it becomes similar to that of SLG for angles ≥ 10° due to the increased decoupling between the two graphene layers. Furthermore, an additional peak (R') is observed at low interlayer rotation angles (3-8°) due to activating the intralayer LO phonon modes and disappears when the interlayer mismatch increases [125, 126]. At higher twist angles (>10°), another peak (R) is activated which corresponds to intervalley TO phonon modes [127, 128]. The position of the R peak is blue shifted as the twist angle increases, as indicated in Figure 4-5b. The G-peak enhancement noticed at 11-12° is due to matching between the laser excitation energy and the energy splitting between van-Hove singularities [129]. The critical angle (θ_{cr}) at which the G-peak enhancement occurs can be calculated by [129]:

$$E_{laser} = \frac{8\pi}{3\alpha} \hbar \, v_f \, sin\left(\frac{\theta_{cr}}{2}\right) \qquad (4\text{-}2),$$

where α=2.46Å is the lattice constant, E_{laser} is the laser energy, $\hbar$ is the reduced Planck's constant, v_f = 10^6 m/s is the Fermi velocity. For a 532 nm laser, θ_{cr} =11° which agrees with the data shown in Figure 4-5b. For twist angles > 13º, Raman spectrum becomes similar to SLG, signifying the decoupling between the graphene layers.

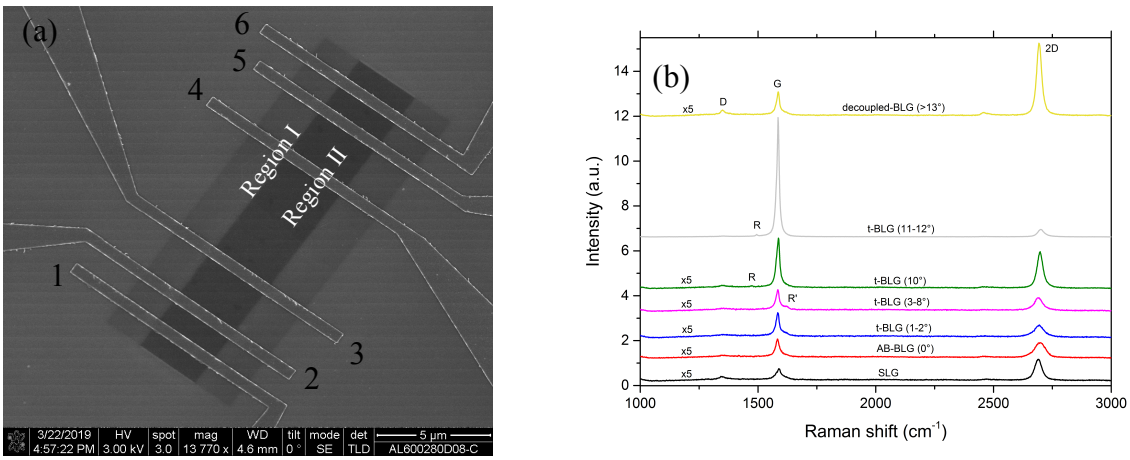


Figure 4-5: (a) SEM image of a typical fabricated device, (b) Raman spectra of SLG as well as BLG with different stacking angles. All Raman signals except for 11-12° case are multiplied by a factor of five to better visualize the peaks

To extract the interlayer resistivity, four probe measurements were employed and the resistance between each pair of contacts is obtained as shown in Figure 4-6a. Note that there is a redundancy between some of the measurements to make sure that the resistance measured between any two pads truly represents the intrinsic graphene's resistance. For example, R1-6-4-5, which corresponds to sourcing current between contacts 1 and 6 and sensing the voltage between contacts 4 and 5, should give the same resistance as R3-6-4-5, which is confirmed from Figure 4-6a. Furthermore, Figure 4-6a shows that the Dirac point is very close to zero, indicating a negligible unintentional doping from oxygen and water molecules. The average field effect mobility of BLG with different twist angles normalized to SLG is shown in Figure 4-6b. The average mobility of SLG is ~1,900 $cm^2/V.s$, extracted 30V away from the Dirac point which corresponds to a carrier concentration of $\sim 7\times10^{12}$ cm^{-2}. AB-stacked BLG has lower mobility compared to SLG due to the parabolic band structure of bilayer graphene as opposed to the linear dispersion in single layer graphene [130, 131]. On the other hand, twisted BLG

is characterized with a relatively higher mobility due to the decoupling between the graphene layers, which changes its band structure, eventually leading to a linear band structure at high twist angles. The mobility monotonically increases with increasing the twist angle, in agreement with the results shown in [132].

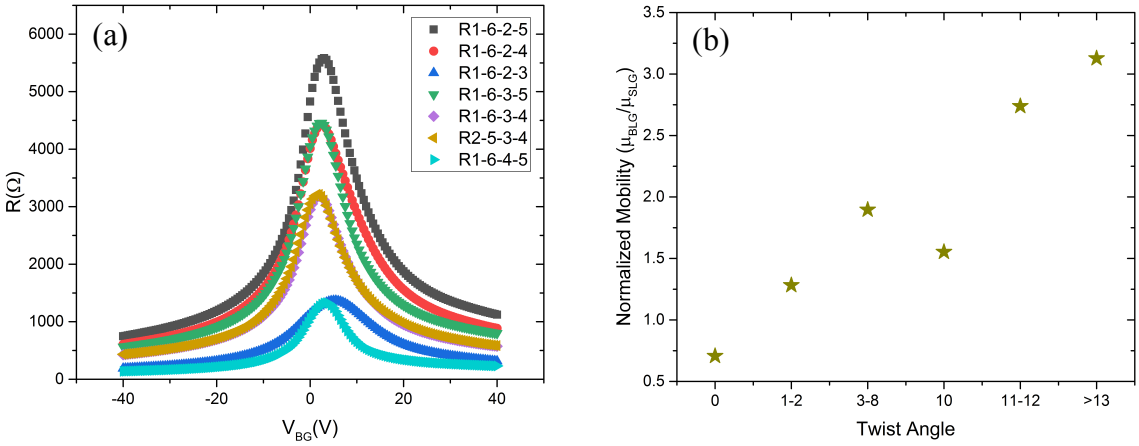


Figure 4-6: (a) Four probe measurement of the resistance between source (S) and drain (D) versus back-gate voltage for several contact pairs along graphene. Note that for the same sensing contacts, changing the sourcing contacts does not change the measured resistance, emphasizing the consistency of the measurements. Note also that the Dirac point is very close to zero, indicating a minimum unintentional doping. (b) Average field-effect mobility of BLG with different twist angles normalized to SLG. AB-stacked BLG has lower mobility than SLG due to parabolic band structure whereas twisted BLG has higher mobility than SLG due to decoupling between the layers

4.5 Extraction of Interlayer Resistivity in Multilayer Graphene

Most of the previous reports used a lumped resistance network to model multilayer graphene interconnects [67, 69, 73]. A lumped model cannot precisely capture the current distribution in the middle of few-microns-long interconnects, leading to an inaccurate extraction of the interlayer resistivity. To properly extract the interlayer

resistivity value from the experimental data, we developed a distributed resistance network model to simulate the resistance between any two contacts on the sample. The circuit-level schematic for a stepped graphene is shown in Figure 4-8a. The in-layer segment resistance on the i^{th} graphene layer is calculated as:

$$r_i = R_{sheet,i} \times \frac{dl}{W} \quad (4\text{-}3),$$

where $R_{sheet,i}$ is the sheet resistance on the i^{th} layer, dl is the segment length, and W is the width of the graphene. The interlayer segment resistance is calculated as:

$$r_{int} = \rho_c \times \frac{d_{int}}{W \times dl} \quad (4\text{-}4),$$

where ρ_c is the interlayer resistivity and $d_{int} = 0.35\text{nm}$ is the distance between two graphene layers. By setting input/output current sources and solving Kirchhoff's Current Law at each circuit node, all voltages and currents can be obtained for the entire network. The simulation framework is highly flexible, and one can define all the important parameters, such as the number of graphene layers on each side of the step, the location of four contacts in the experiments, etc.

The sheet resistance of the bottom graphene layer can be directly extracted from experiments by measuring the resistance between Pad2 and Pad3 whereas the interlayer resistivity as well as the top layer sheet resistance are kept as fitting parameters in the model. The resistance between each pad pair as a function of the back-gate voltage as

well as the sheet resistance of the bottom graphene layer are fed into the model and the values of the fitting parameters are chosen such that the error between the simulated and experimental resistance values throughout the whole back-gate voltage sweep is minimized. Figure 4-8b compares the measured resistance between Pad2 and Pad5 and the simulated one, showing an average error less than 5% throughout the whole back-gate voltage sweep. This ensures the accuracy of the model used.

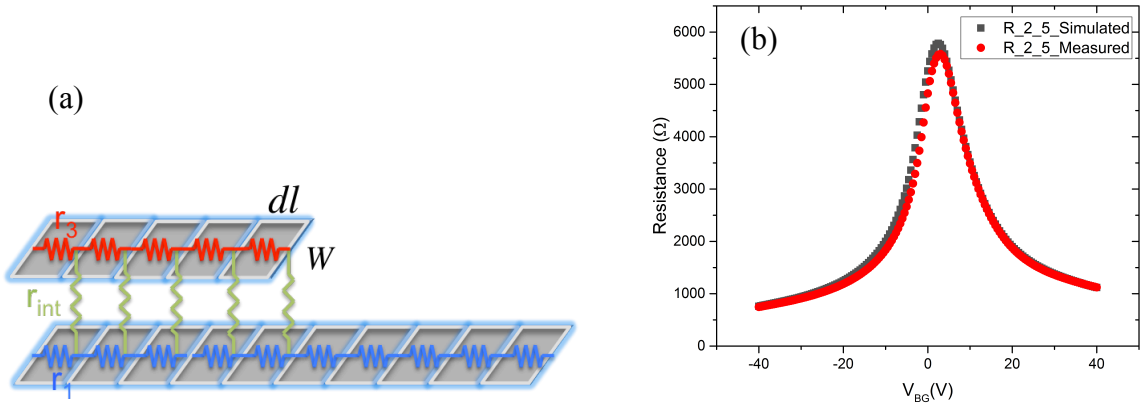


Figure 4-7: (a) Circuit-level schematic of the fabricated stepped graphene structure, (b) Comparison between the experimentally measured resistance between Pad2 and Pad5 and its simulated counterpart showing a very good agreement between the experiment and the model

Figure 4-8a shows the extracted interlayer resistivity of BLG with different twist angles as a function of the back-gate voltage. For AB-stacked BLG, the interlayer resistivity varies from ~140 Ω.m at a back-gate voltage of 5V away from the Dirac point to ~45 Ω.m at 25V. On the other hand, twisted bilayer graphene shows an interlayer resistivity as low as 40 Ω.m at 5V and 6 Ω.m at 25V, with the interlayer resistivity generally decreasing as increasing the twist angle. However, the plot corresponding to a twist angle of 1-2º shows a relatively lower interlayer resistivity compared to that of 3-8º

and 10º. This can be understood by comparing the defect density in the 1-2º twist angle case with that of 3-8º and 10º. The point defect density in graphene can be quantified as:

$$n_D(cm^{-2}) = \frac{(1.8 \pm 0.5)\times 10^{22}}{\lambda_L^4}\left(\frac{I_D}{I_G}\right) \quad (4\text{-}5),$$

where λ_L is the Raman excitation wavelength (in nanometers). Using equation (4-5) together with Figure 4-5b, the sample with 1-2º twist angle has the highest defect density of $1.2\text{x}10^{10}$ cm^{-2} compared to 3-8º and 10º twist angle cases that have defect densities of $9\text{x}10^{9}$ cm^{-2} and $4.5\text{x}10^{9}$ cm^{-2}, respectively. These lattice defects may enhance the electronic coupling between layers, as suggested by Kempa *et al.* [133] giving rise to a relatively lower interlayer resistivity for the 1-2º twist angle case.

The extracted interlayer resistivity for AB-stacked BLG is 2-5 orders of magnitude higher than the previously reported values for graphite. However, we believe that comparing the interlayer conduction of graphene with that of AB-stacked graphite is not an accurate comparison since they have different band structures and effective masses. Also the measurement technique adopted in earlier reports might not be accurate, as outlined earlier in this chapter.

More interestingly, twisted graphene showed 3-5x lower interlayer resistivity compared to its AB-stacked counterpart. This trend is in contrast to the predictions of earlier reports [75, 134, 135] which predicted that interlayer conduction is suppressed by momentum conservation whenever the layer stacking has a rotation, leading to an interlayer resistivity that is four orders of magnitude higher than that of AB-stacked

graphite. Later on, this theory was revisited and it was suggested that phonon scattering can provide the momentum change required for interlayer conduction. However, it was shown that phonon-mediated conduction decays with increasing the twist angle [135], which should lead to a relatively larger interlayer resistivity in BLG samples with large twist angles as compared to those with lower twist angles. Nevertheless, we notice an opposite trend in Figure 4-8a. This suggests that a different conduction mechanism is responsible for interlayer conduction in twisted graphene. However, this phenomenon needs to be studied in further details and it is not the focus of this work.

Figure 4-8b indicates that the sheet resistance of the top graphene layer in twisted BLG is much smaller than that of its AB-stacked counterpart. This is due to the decoupling between the two graphene layers which improves the carrier mobility as confirmed by Figure 4-6b. Furthermore, the interlayer resistivity decreases with increasing the number of graphene layers for both AB-stacked and decoupled graphene as shown in Figure 4-8c and Figure 4-8d, respectively. This suggests that the interlayer conduction is affected by the coupling between all the graphene layers in the stack rather than layer-to-layer coupling. It may also partially explain why the reported interlayer resistivity in graphite (which is formed from a few-thousands graphene layers stack) is much smaller than the value we obtained for few-layer graphene. However, one should still note that graphene and graphite are two different materials and a direct comparison between them should be considered with great care as pointed out earlier.

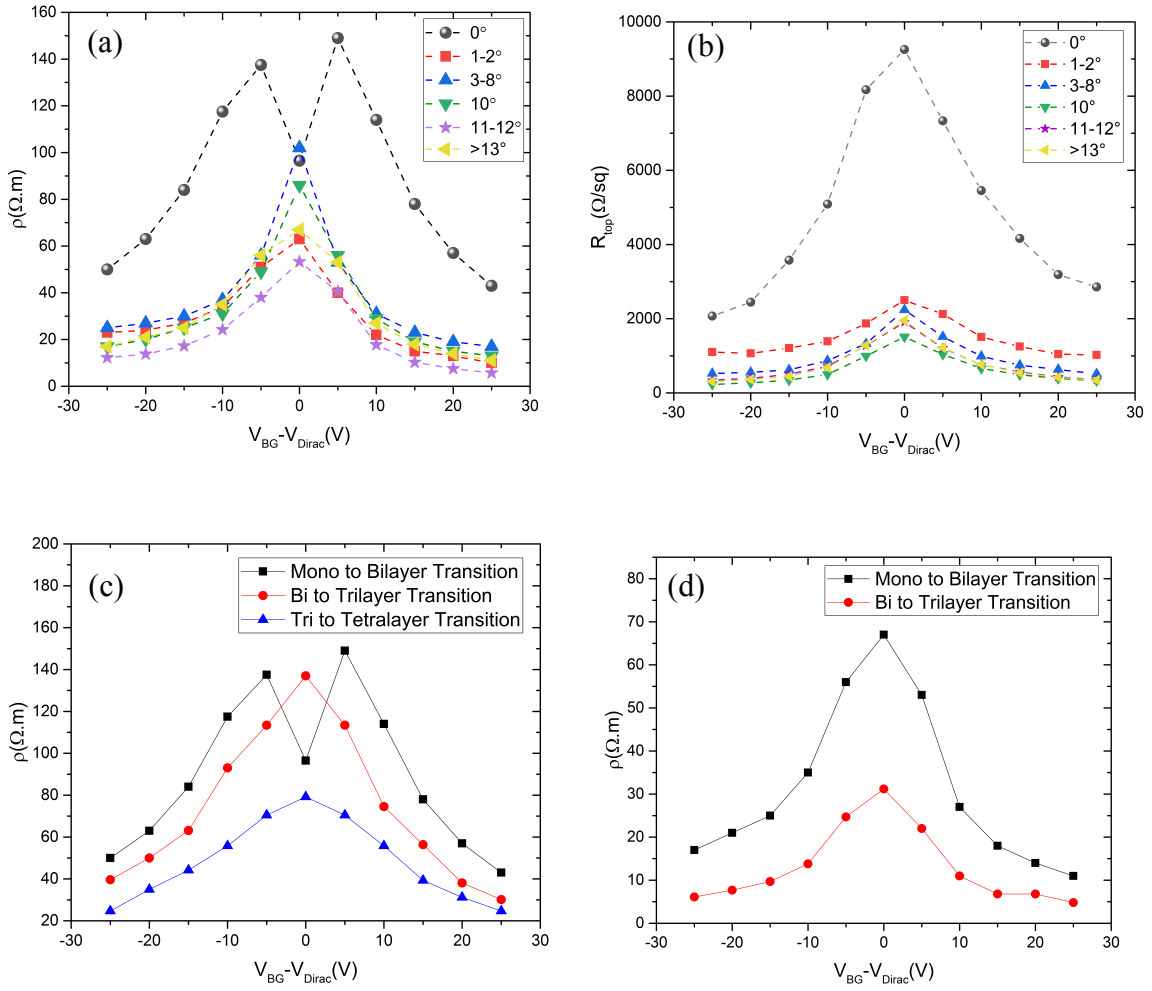


Figure 4-8: (a) Interlayer resistivity as a function of back-gate voltage of BLG with different twist angles showing a 3-5x lower interlayer resistivity in the twisted case compared to the AB-stacked case, (b) Sheet resistance of the top graphene layer as a function of back-gate voltage in BLG with different twist angles showing up to 8x lower resistance in twisted BLG compared to AB-stacked counterpart due to improved carrier mobility, (c) Interlayer resistivity of AB-stacked graphene as a function of back-gate voltage up to four graphene layers, (d) Interlayer resistivity of decoupled (twist angle>13°) graphene up to three layers.

4.6 Electrical Performance of Bilayer Graphene Interconnects

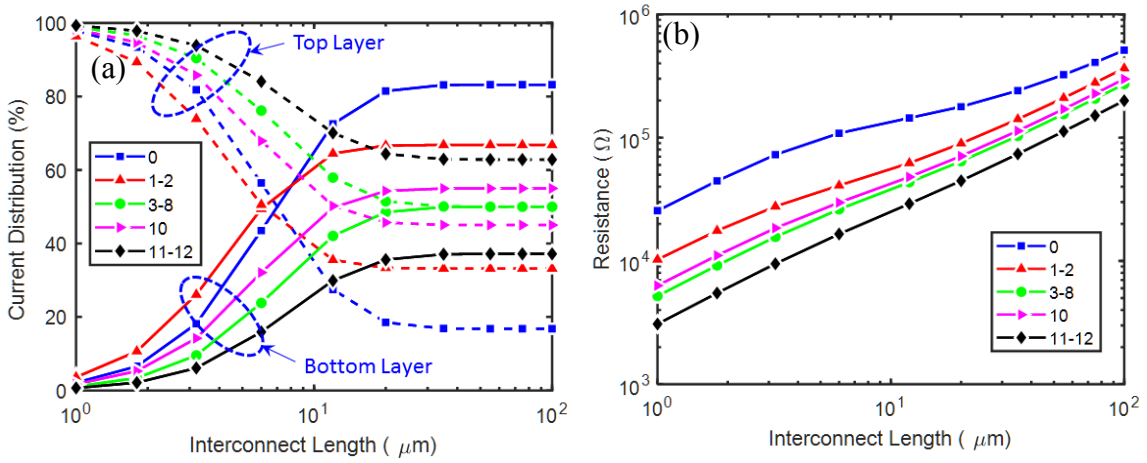
Figure 4-9a shows the current distribution of bilayer graphene interconnects as a function of length for different twist angles between the graphene layers. It is clear that the current predominantly flows in the top layer for interconnect lengths less than a few

micrometers. This is in contrast to the findings of Das and Appenzeller who studied the current distribution of 13-layer graphene system and reported that the current predominantly flows through the bottom layers [136]. The main reason behind this discrepancy is that Das and Appenzeller assumed an interlayer resistivity of 10^{-4} Ω.m whereas the lowest interlayer resistivity we extracted is ~ 10 Ω.m. This relatively large interlayer resistivity makes it difficult for the current to flow to the bottom layer and thereby forces the current to predominantly reside in the top layer. Furthermore, due to the relatively short screening length of graphene (~0.6nm), the carrier concentration in the top layers of the 13-layer graphene system is very small, making the top layers highly resistive compared to the bottom layers, hence driving the current to the bottom layers. Since the resistance of the top layer in twisted graphene is significantly smaller than that of AB-stacked graphene (Figure 4-8b), the total resistance of twisted graphene is about one order of magnitude less than that of its AB-stacked counterpart, as shown in Figure 4-9b.

As the interconnect length is increased beyond 10μm, the current starts to redistribute between the two graphene layers where it saturates for interconnects longer than 20 μm. For top-contacted AB-stacked BLG, 80% of the current flows in the bottom layer for sufficiently long interconnects (>20 μm) whereas only 35% of the total current flows in the bottom layer for 11-12° twisted graphene. This is because in case of AB-stacked graphene, the top layer has a much higher resistance than the bottom layer whereas for 11-12° twisted graphene the top- and bottom-layer resistances are comparable, as shown in Figure 4-9c. This forces the current to flow to the less resistive bottom layer in case of AB-stacked graphene, despite the relatively high interlayer

resistivity. As a result, the total resistance of AB-stacked BLG is more comparable to that of twisted graphene for interconnect lengths beyond 20μm.

Since the top-layer sheet resistance is smaller than its lower-layer counterpart for 11-12° twisted BLG, the total resistance of a few μm-long top-contacted 11-12° twisted BLG is smaller than its bottom-contacted counterpart as illustrated in Figure 4-9d. This is because for short interconnect lengths, the current predominantly flows in the layer that is coupled directly to the contact. As the interconnect length increases, the current starts to redistribute between the two layers until it eventually saturates for both contact configurations, leading to the same total resistance regardless of the contact configuration.



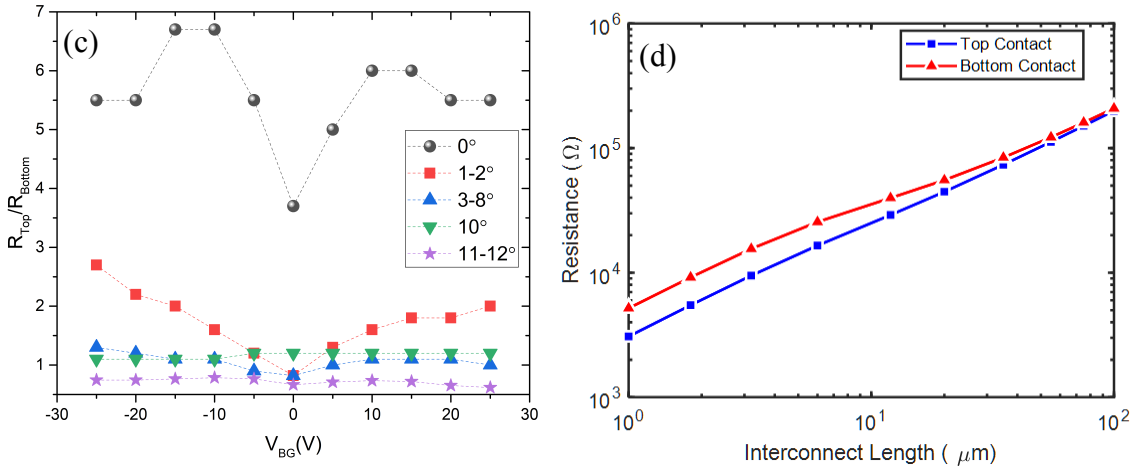


Figure 4-9: (a) Current distribution and (b) Total resistance in BLG interconnects as a function of length for different twist angles, (c) Ratio between top layer resistance (R_{Top}) and bottom layer resistance (R_{Bottom}) in BLG extracted from four-probe measurements as a function of backgate voltage for different twist angles showing $R_{Top}/R_{Bottom}>1$ for AB-stacked graphene and $R_{Top}/R_{Bottom}<1$ for 12° twisted graphene, (d) Total resistance of 12° twisted BLG graphene using Top- and Bottom-contacts. Note that for relatively short interconnects, top-contacted interconnects show up to 2x reduction in total resistance.

To assess the performance of BLG as a potential candidate for interconnect applications, the RC delay (t_{delay}) as well as the energy dissipation (E_{diss}) of BLG interconnects as a function of number of graphene layers are calculated as:

$$t_{delay} = 0.7\, R_0\, (C_0 + c_w) + 0.4\, r_w\, c_w + 0.7\, r_w \qquad (4\text{-}6),$$

$$E_{diss.} = \frac{1}{2}\, (C_0 + c_w)\, V_{DD}^2 \qquad (4\text{-}7),$$

where r_w is the graphene's resistance calculated based on the experimental values given in Figure 4-9, c_w is graphene's capacitance which is the series combination of quantum and electrostatic capacitances whose values were adopted from previous work [137], R_0 and C_0 are the driver/load resistance and capacitance, respectively, and V_{DD} is the supply voltage. In these simulations, the wire width is 100nm, the sheet resistance is extracted by performing the fitting based on experimental measurements, and the technology for the transistor is at the 15nm node with fan out of 3.

Figure 4-10a, b show the delay and energy-delay product (EDP) of BLG interconnects with different stacking angles as a function of interconnect length. Twisted BLG tends to have lower delay and EDP compared to AB-stacked graphene, with 11-12° twisted graphene showing the lowest delay and EDP. This is because twisted graphene has lower total resistance compared to its AB-stacked counterpart, as illustrated earlier in Figure 4-9b. As the interconnect length increases, both the delay and EDP increase due to larger resistance and capacitance values. It is worth mentioning that the value of the capacitance is based on the calculated values of quantum and electrostatic capacitances where it was assumed that their respective values do not depend on the stacking angle. This assumption might not be accurate and hence an experimental verification of the exact MLG capacitance values for different stacking orientation might be needed.

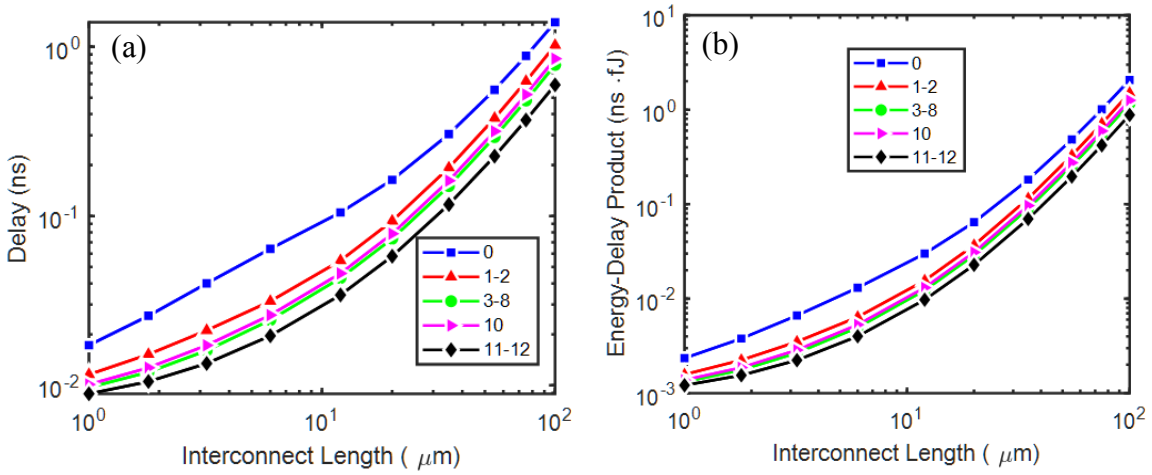


Figure 4-10: (a) Delay and (b) Energy-Delay Product of BLG interconnect as a function of interconnect length.

4.7 Conclusion

We have proposed an accurate method to determine the interlayer resistivity of top-contacted two-dimensional layered systems based on the direct measurement of the resistance at a mono-to-bilayer step and feeding the measured resistance to a distributed resistance model to extract the interlayer resistivity. We used CVD-grown graphene as an example to illustrate our method. The interlayer resistivity of CVD-grown AB-stacked bilayer graphene was found to be in the range of 50-140 $\Omega \cdot$m, which is two-five orders of magnitude larger than the previously reported values for AB-stacked graphite. This discrepancy with previous reports can possibly be because of the measurement technique used which tends to alter the band structure, and consequently the effective mass, of graphene/graphite. Also, previous experiments were mostly conducted on thick pieces of graphite which has a different band structure from that of graphene. On the other hand,

twisted BLG shows 3-5x lower interlayer resistivity compared to AB-stacked BLG with the interlayer resistivity monotonically decreasing with increasing the twist angle. This suggests that interlayer conduction is not limited by phonon scattering, as previously reported, and hence the theory behind interlayer conduction in twisted graphene needs to be refined. Furthermore, we found that the interlayer resistivity of MLG monotonically decreases with increasing the number of graphene layers.

In addition, we show that for top-contacted graphene, the current predominantly flows in the top graphene layer for relatively short interconnect lengths (less than a few micrometers) whereas current starts to distribute among the graphene layers according to the resistance of each layer for interconnects longer than 20 μm. The total resistance of twisted BLG was found to be about one order of magnitude lower than its AB-stacked counterpart, leading to a lower delay and energy-delay product in twisted graphene. This suggests that twisted BLG with large twist angles is a more promising interconnect material compared to its AB-stacked counterpart.

CHAPTER 5. CONCLUDING REMARKS AND FUTURE RESEARCH

5.1 3D-NAND Flash Memory

In this thesis it was shown that graphene can enhance the electric field in floating-gate 2D NAND, leading to a lower write voltage and/or lower programming time. Even though in principle this can be applied to state-of-the-art 3D NAND memory technology, experiments still need to be conducted to verify the benefits of incorporating graphene in 3D NAND. Integrating graphene into the fabrication process flow of 3D NAND can be very challenging since it currently requires transferring graphene from the metal foil, usually Cu or Ni, on which it is grown to the 3D NAND memory holes. One way to circumvent this challenge is to grow graphene directly on SiO_2, which was already reported by some groups. However, the quality of the grown graphene needs to be improved. Another solution might be to consider metal/graphene heterostructures and extract their field enhancement factor.

5.2 Interlayer Resistivity of 2D materials

In this thesis, an accurate method was proposed to measure the interlayer resistivity of 2D materials. While the interlayer resistivity of multilayer graphene was thoroughly studied as a function of number of graphene layers and stacking orientation, some interesting cases were not studied due to time limitations. For example, intercalated graphene represents a promising candidate for electrical interconnects due to its lower resistivity. However, a detailed study of the interlayer resistance and the role of the

intercalant in coupling between the graphene layers is still missing. Furthermore, other 2D materials systems such as metal dichalcogenides are being considered for several electronic applications and understanding the interlayer resistance in these systems can help explore their potential.

5.3 Determination of High Frequency Impedance Parameters in CVD Graphene

The high frequency response of graphene interconnects needs to be studied to assess its performance in high frequency applications. Despite the numerous experimental reports on the DC performance of graphene interconnects, reports describing its high frequency response have been very limited [138-140]. Several analytical models were proposed to better understand the physical and circuit-based elements affecting the performance of MLG interconnects at high frequency [141-143]. However, in these models, the inlayer scattering resistance, the kinetic inductance, and the quantum capacitance are assumed to be equal in all the graphene layers [141, 143, 144], which might not be an accurate assumption since these parameters are functions of the Fermi energy which is different for different graphene layers due to screening. In fact, it was shown in Chapter 4 that bilayer graphene has unequal top and bottom inlayer resistances and that the ratio between these resistances depend on the stacking orientation. This suggests that experimentally verified models are needed to accurately analyze the frequency response of MLG interconnects.

Here, two different test structures are proposed from which high frequency circuit components such as interlayer capacitance, quantum capacitance, and kinetic inductance

can be extracted, allowing for an accurate analysis of the frequency response in MLG interconnects.

5.3.1 Design and Experimental Details of Test Structures for High Frequency Analysis in Multilayer Graphene

Two different test structures are tried in order to extract the high frequency interlayer impedance of bilayer graphene (BLG). The first structure is based on a microstrip design and is shown in Figure 5-1a. Here, 20µm wide BLG strips of lengths 50-100µm are etched and serve as the medium through which the signal is driven. The contact area between graphene and the signal pads is 10µm x 10µm. The ground pads are deposited directly on SiO_2. The microstrips are made with different lengths to eliminate the length-dependent component of the measured impedance and hence extract the intrinsic impedance values. Furthermore, standard OPEN, SHORT, and THRU patterns are fabricated next to each graphene microstrip to de-embed the parasitics of the pads and interconnects. The de-embedding structures are made the same size as that on the graphene to ensure accurate de-embedding.

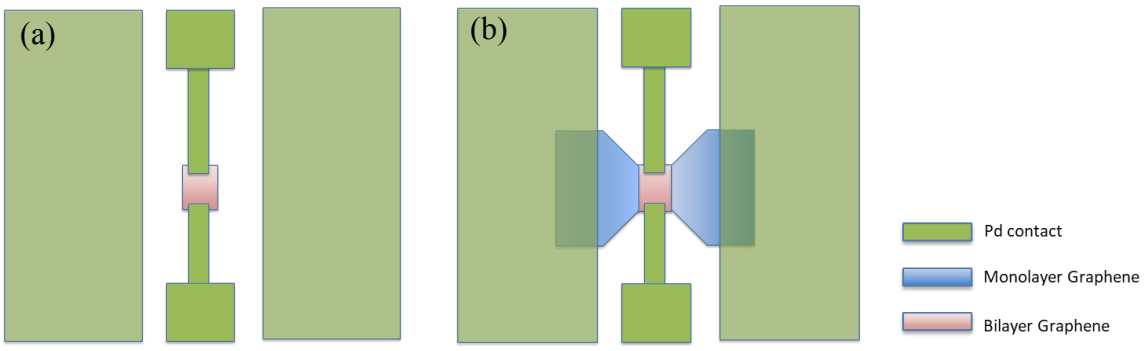


Figure 5-1: (a) Microstrip structure, (b) Coplanar Waveguide structure to extract the interlayer impedance of graphene

Figure 5-1b shows the second test structure, which is based on a Coplanar Wave Guide (CPW) configuration. In this case, an area containing a BLG region sandwiched between two single-layer graphene (SLG) regions is etched where the ground pads are deposited on the SLG regions and the BLG region is the medium through which the signal is driven. The contact area between SLG and the ground pads is maximized to ensure a low contact resistance. The contact area between BLG and the signal pads is 10μm x 10μm, same as in the microstrip structure. CPWs are designed with different dimensions, as in the case of microstrip design. However, the dimensions are not well-controlled in this case since they depend on the geometry of the mono-bi-monolayer graphene patches. Standard OPEN, SHORT, and THRU patterns are fabricated next to each graphene CPW to de-embed the parasitics of the pads and interconnects.

5.3.2 Microstrip and CPW Device Fabrication

Graphene growth and transfer are conducted as given in Section 4.3.1 of Chapter 4. Microstrip and CPW structures are fabricated on the same sample using the same lithography steps. First, graphene was patterned using Electron Beam Lithography (EBL) where a film of 2% Hydrogen Silsesquioxane (HSQ) is spin-coated at 4000rpm for 60s with a 3s ramp on top of a PMMA 3C film spin-coated at 4500rpm for 60s with a 3s ramp. After EBL exposure, the sample is developed in OPD5262 for 60s followed by DI water rinse and N_2 blow drying. The sample is then subjected to a 100W O_2 plasma for 8 minutes to etch the graphene that is not protected by the HSQ. The PMMA layer acts as a sacrificial layer to protect the underlying graphene from the damage that would occur if the HSQ layer were to be removed by plasma etching. The PMMA/HSQ resist stack can be removed by leaving the sample in hot acetone (at 50 °C) for two hours followed by

IPA rinse. A second EBL step is employed to create the metal contacts where the sample is firstly prebaked at 120°C on a hotplate for 5 minutes. After that, a PMMA in 3% chlorobenzene resist is applied to the sample by spin coating at 4500rpm for 45s. After EBL exposure, the sample is developed in 1:1 MIBK:IPA for 50s followed by a 30s IPA dipping. 50nm thick Pd contacts are deposited using e-beam evaporation followed by an overnight liftoff process in hot acetone.

5.3.3 Microstrip and CPW Device Characterization

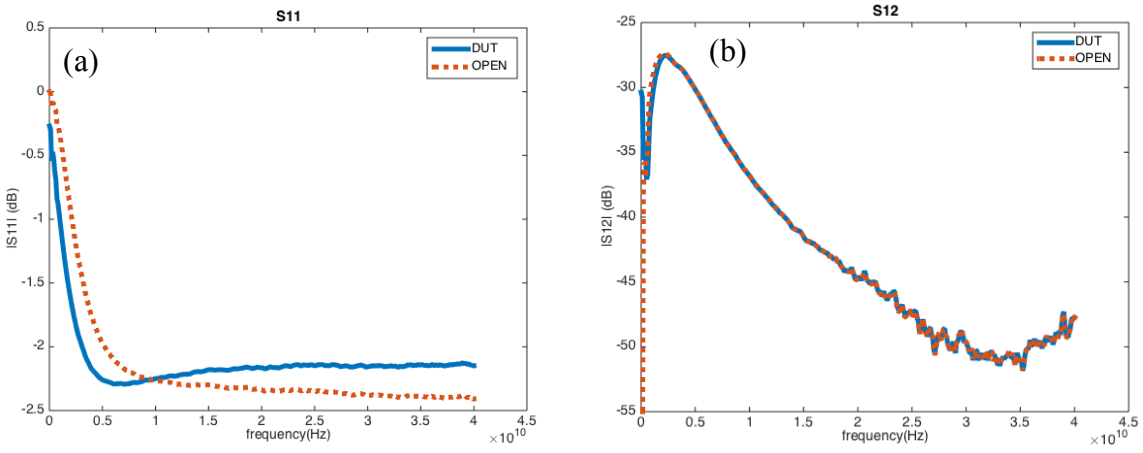
Two-port high frequency measurements from 100MHz to 40GHz were performed using Vector Network Analyzer (VNA) and GSG configuration probes. Prior to measurement, standard SHORT, OPEN, LOAD, THRU (SOLT) calibration was done to eliminate system errors from the VNA and account for the loss caused by the coaxial cables and the probes. The conventional open-short de-embedding technique is used to eliminate the series and parallel parasitics and hence extract the intrinsic parameters of BLG, according to the equation [145]:

$$Y_{BLG} = ((Y_{DUT} - Y_{OPEN})^{-1} - (Y_{SHORT} - Y_{OPEN})^{-1})^{-1} \quad (5\text{-}1),$$

where Y_{BLG} is the intrinsic admittance of BLG device, Y_{DUT} is the admittance of the device under test before de-embedding, and Y_{OPEN} and Y_{SHORT} are the admittances of the OPEN and SHORT standards, respectively.

5.3.4 Preliminary Experimental Results

Figure 5-2 compares the S-parameters of the graphene microstrip with that of the OPEN standard. It is clear that the graphene microstrip behaves as an open circuit over the whole frequency range considered. This could be due to the high resistance of the relatively long graphene strip and/or the contact resistance at the graphene/metal interface. In order to extract the intrinsic high frequency graphene impedance, shorter graphene strips may need to be fabricated and the contact area between the graphene and the metal pad may need to be maximized.



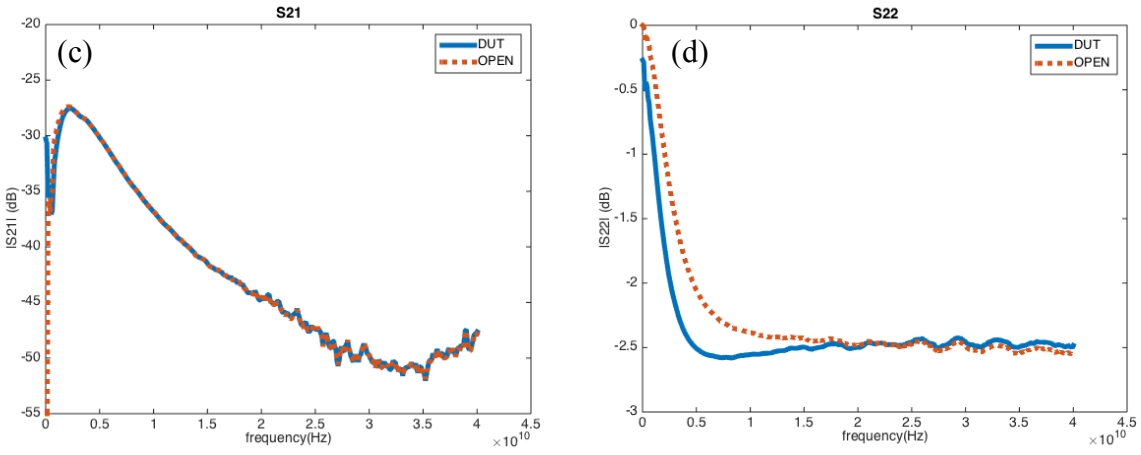


Figure 5-2: S-Parameters of a 100µm x 20µm microstrip BLG together with the corresponding OPEN standard showing that microstrip BLG essentially behaves as an open circuit

Figure 5-3a illustrates the extracted Y12 parameter of the CPW structure before and after de-embedding together with Y12 of SHORT and OPEN de-embedding structures. It is clear that after de-embedding, the intrinsic Y12 of graphene is very small. This is probably due to the relatively large input pad capacitance of ~ 1pF, shown in Figure 5-3b, which dominates the measured impedance. Unfortunately, this high input pad capacitance impedes the extraction of intrinsic graphene impedance.

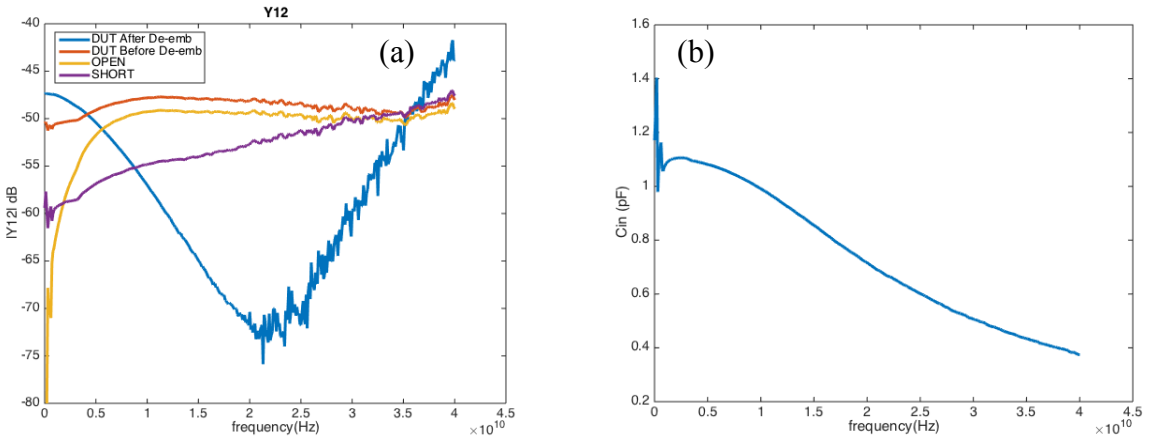


Figure 5-3: (a) Y12 of the CPW structure before and after de-embedding together with Y12 of SHORT and OPEN de-embedding structures, (b) Input capacitance of the CPW structure

5.4 Conclusion of Dissertation

In this thesis we studied CVD-grown graphene as a potential candidate for memory as well as electrical interconnect applications. The continuous increase in the 3D memory density required an increase in the height of the 3D stack. This, in turn, dictated an increase in the width of the memory hole which is accompanied by a reduction in the electric field inside the memory hole. To compensate for the reduced electric field, an increase in the programming voltage and/or programming time is required at the expense of higher power dissipation and/or slower memory operation. Furthermore, with the continuous scaling of feature size, interconnects become the dominating factor in determining the performance of electronic circuits due to increased RC delay of interconnects, increased crosstalk between nearby interconnect lines, increased dynamic power dissipation, and reliability issues due to electromigration. Graphene can

compensate for the reduced electric field in 3D memory devices while keeping the programming voltage sufficiently low by enhancing the electric field at its atomically-thin, sharp edges. Also, graphene is considered a promising alternative to copper interconnects owing to its current carrying capability that can reach 10^8 A/cm^2 [1], ultrahigh intrinsic carrier mobility [2], and low resistivity [3].

In Chapter 2, we extracted an average field-enhancement factor (β) of ~2.06 with a standard deviation of 0.33 for CVD-grown single layer graphene based on an MOS structure. This modest value solves the contradiction in prior experiments that reported a field enhancement factor of few thousands but only 30-40% improvement in the write voltage of floating gate memory devices. We have used a modified Fowler-Nordheim (FN) model that is applicable to 2D materials to extract the field enhancement factor of graphene and compared the results to that obtained from the conventional FN model. We found that the conventional FN model tends to slightly overestimate the value of β by about 30% compared to the modified FN model. This suggests that the overestimated β values reported previously are not caused by the extraction method and could be stemming from the fact that in earlier experiments graphene was deposited on metals whose work functions have a large mismatch (1.5-2 eV) with that of graphene, which in turn shifts the Fermi energy and lowers the barrier for tunneling. In addition to that, previous reports used air as the tunneling dielectric, which is leakier than SiO_2 due to its low dielectric constant. The experimentally extracted β value was used to drive higher-level circuit simulations on 64-bit NAND strings and it was shown that 2D NAND programming time and/or programming voltage can be suppressed to 10ns and 5V, respectively, based on a 65 nm process node.

In Chapter 3, CVD-grown single layer graphene is studied as a potential candidate for electrical interconnect applications. A simple two-step lithography process to fabricate graphene devices with mobilities up to ~9,500 $cm^2/V.s$ at a carrier concentration of $4x10^{12}$ cm^{-2} has been presented. The high quality of these devices is attributed to the presence of an HSQ pinning dielectric that is applied immediately after the transfer step. This dielectric anchors the loosely bound graphene sheet to the SiO_2 surfaces, primarily screening local charged impurities and secondarily reducing process damage. The potential benefits of graphene interconnects are evaluated based on the MFP extracted from the experimental data. Even though the reported mobility is more than 2x higher than the average recorded mobility, MFP analysis shows that the MFP attained still needs to at least be doubled in order to achieve a significant improvement in the energy-delay product over copper interconnects. This means that we should further improve the mobility to reach around 20,000 $cm^2/V.s$. Possible methods to achieve such a high mobility are to optimize the dielectric constant of HSQ and/or replace the SiO_2 underneath graphene with a high-k dielectric. Also, better performance can be achieved by considering multilayer graphene instead of single layer graphene.

In Chapter 4, we propose an accurate method to determine the interlayer resistivity of MLG based on the direct measurement of the resistance at a mono-to-bi layer step and feeding the measured resistance to a distributed resistance model to extract the interlayer resistivity. The extracted values were used to analyze the performance of MLG interconnects in terms of interconnect delay, energy dissipation, and energy-delay product. MLG with up to 4 graphene layers and different stacking orientations were studied. The interlayer resistivity of CVD-grown AB-stacked bilayer graphene was found

to be in the range of 50-140 Ω·m, which is two-five orders of magnitude larger than the previously reported values for AB-stacked graphite. This discrepancy with previous reports is mainly because of the measurement technique used earlier, which tends to alter the band structure, and consequently the effective mass, of graphene/graphite. Also previous experiments were mainly conducted on thick pieces of graphite which has a different band structure than that of graphene. On the other hand, twisted BLG shows 3-5x lower interlayer resistivity compared to AB-stacked BLG with the interlayer resistivity monotonically decreasing with increasing the twist angle. This suggests that interlayer conduction is not limited by phonon scattering, as previously reported, and hence the theory behind interlayer conduction in twisted graphene needs to be refined. Furthermore, we found that the interlayer resistivity of MLG monotonically decreases with increasing the number of graphene layers. In addition, we show that the current predominantly flows in the top graphene layer for relatively short interconnect lengths (less than 10μm) whereas current starts to distribute among the graphene layers for interconnects longer than 10μm, with an optimum current distribution beyond 20 μm. The total resistance of twisted BLG was found to be about one order of magnitude lower than its AB-stacked counterpart, leading to a lower delay and energy-delay product in twisted graphene. The proposed method used to extract the interlayer resistivity is generic and can be applied to other 2D systems such as metal dichalcogenides. Also the same analysis technique can be applied to intercalated MLG in order to better analyze its performance as a potential candidate for electrical interconnect applications.

REFERENCES

1. Avouris, P., Z. Chen, and V. Perebeinos, *Carbon-based electronics.* Nature nanotechnology, 2007. **2**(10): p. 605-615.

2. Bolotin, K.I., et al., *Ultrahigh electron mobility in suspended graphene.* Solid State Communications, 2008. **146**(9-10): p. 351-355.

3. Novoselov, K.S., et al., *Electric field effect in atomically thin carbon films.* Science, 2004. **306**(5696): p. 666-669.

4. Moore, G.E., *No exponential is forever: But "forever" can be delayed!* 2003 Ieee International Solid-State Circuits Conference: Digest of Technical Papers, 2003. **46**: p. 20-23.

5. Chau, R., et al., *High-kappa/metal-gate stack and its MOSFET characteristics.* Ieee Electron Device Letters, 2004. **25**(6): p. 408-410.

6. Xuejue, H., et al. *Sub 50-nm FinFET: PMOS.* in *Electron Devices Meeting, 1999. IEDM '99. Technical Digest. International*. 1999.

7. Chau, R., et al., *Advanced depleted-substrate transistors: single-gate, double-gate and tri-gate.* Solid State Devices and Materials, 2002: p. 68-69.

8. Service, R.F., *Is Silicon's Reign Nearing Its End?* Science, 2009. **323**(5917): p. 1000-1002.

9. Radamson, H. and L. Thylén, *Chapter 4 - Moore's Law for Photonics and Electronics*, in *Monolithic Nanoscale Photonics–Electronics Integration in Silicon and Other Group IV Elements*, H. Radamson and L. Thylén, Editors. 2015, Academic Press: Oxford. p. 121-150.

10. Bondavalli, P., *6 - Graphene, Microelectronics/Nanoelectronics, and More Than Moore*, in *Graphene and Related Nanomaterials*, P. Bondavalli, Editor. 2018, Elsevier. p. 157-169.

11. Yan, C., J.H. Cho, and J.H. Ahn, *Graphene-based flexible and stretchable thin film transistors.* Nanoscale, 2012. **4**(16): p. 4870-4882.

12. Jang, H., et al., *Graphene-Based Flexible and Stretchable Electronics.* Advanced Materials, 2016. **28**(22): p. 4184-4202.

13. Guerriero, E., et al., *Graphene Audio Voltage Amplifier.* Small, 2012. **8**(3): p. 357-361.

14. Kedzierski, J., et al., *Graphene-on-Insulator Transistors Made Using C on Ni Chemical-Vapor Deposition.* Ieee Electron Device Letters, 2009. **30**(7): p. 745-747.

15. Ohno, Y., et al., *Top-gated graphene field-effect transistors by low-temperature synthesized SiNx insulator on SiC substrates.* Japanese Journal of Applied Physics, 2016. **55**(6).

16. Hong, A.J., et al., *Graphene Flash Memory.* Acs Nano, 2011. **5**(10): p. 7812-7817.

17. Hossain, N.M. and M.H. Chowdhury, *Multilayer Graphene Nanoribbon and Carbon Nanotube Based Floating Gate Transistor for Nonvolatile Flash Memory.* Acm Journal on Emerging Technologies in Computing Systems, 2015. **12**(1).

18. Naeemi, A. and J.D. Meindl, *Compact physics-based circuit models for graphene nanoribbon interconnects.* Electron Devices, IEEE Transactions on, 2009. **56**(9): p. 1822-1833.

19. Yang, Y. and R. Murali, *Impact of size effect on graphene nanoribbon transport.* Electron Device Letters, IEEE, 2010. **31**(3): p. 237-239.

20. Xie, G., et al., *Graphene edge lithography.* Nano letters, 2012. **12**(9): p. 4642-4646.

21. Murali, R., et al., *Resistivity of graphene nanoribbon interconnects.* Electron Device Letters, IEEE, 2009. **30**(6): p. 611-613.

22. Ferrari, A.C., et al., *Science and technology roadmap for graphene, related two-dimensional crystals, and hybrid systems.* Nanoscale, 2015. **7**(11): p. 4598-4810.

23. Li, X.S., et al., *Large-Area Synthesis of High-Quality and Uniform Graphene Films on Copper Foils.* Science, 2009. **324**(5932): p. 1312-1314.

24. Bae, S., et al., *Roll-to-roll production of 30-inch graphene films for transparent electrodes.* Nat Nanotechnol, 2010. **5**(8): p. 574-8.

25. Rajkanan, K. *Flash memory technology-A review*. in *Memory Technology, Design and Testing, 1996. Records of the 1996 IEEE International Workshop on*. 1996. IEEE.

26. Wang, X.M., W.G. Xie, and J.B. Xu, *Graphene Based Non-Volatile Memory Devices.* Advanced Materials, 2014. **26**(31): p. 5496-5503.

27. Kolodny, A., et al., *Analysis and Modeling of Floating-Gate Eeprom Cells.* Ieee Transactions on Electron Devices, 1986. **33**(6): p. 835-844.

28. Lu, C.Y., K.Y. Hsieh, and R. Liu, *Future challenges of flash memory technologies.* Microelectronic Engineering, 2009. **86**(3): p. 283-286.

29. Van Houdt, J., *High-K materials for nonvolatile memory applications.* 2005 Ieee International Reliability Physics Symposium Proceedings - 43rd Annual, 2005: p. 234-239.

30. Myung Kwan, C. and D.M. Kim, *High performance SONOS memory cells free of drain turn-on and over-erase: compatibility issue with current flash technology.* IEEE Electron Device Letters, 2000. **21**(8): p. 399-401.

31. White, M.H., et al. *A low voltage SONOS nonvolatile semiconductor memory technology*. in *Proceedings of Nonvolatile Memory Technology Conference*. 1996.

32. Yoon, J.H. and G.A. Tressler, *Advanced flash technology status, scaling trends & implications to enterprise SSD technology enablement.* Flash Memory Summit, 2012. **3**(3.1): p. 4.

33. Jung, S.M., et al., *Three dimensionally stacked NAND flash memory technology using stacking single crystal Si layers on ILD and TANOS structure for beyond 30nm node.* 2006 International Electron Devices Meeting, Vols 1 and 2, 2006: p. 503-+.

34. Lai, E.K., et al., *A multi-layer stackable thin-film transistor (TFT) NAND-Type flash memory.* 2006 International Electron Devices Meeting, Vols 1 and 2, 2006: p. 507-+.

35. Tanaka, H., et al., *Bit cost scalable technology with punch and plug process for ultra high density flash memory.* 2007 Symposium on Vlsi Technology, Digest of Technical Papers, 2007: p. 14-+.

36. Jang, J., et al., *Vertical Cell Array using TCAT(Terabit Cell Array Transistor) Technology for Ultra High Density NAND Flash Memory.* 2009 Symposium on Vlsi Technology, Digest of Technical Papers, 2009: p. 192-+.

37. Aritome, S., et al., *Advanced DC-SF Cell Technology for 3-D NAND Flash.* Ieee Transactions on Electron Devices, 2013. **60**(4): p. 1327-1333.

38. Clarke, P., *Intel, Micron Launch "Bulk-Switching" ReRAM*, in *EE Times*. 2015, AspenCore Media: United States of America.

39. Nitayama, A. and H. Aochi, *Bit Cost Scalable (BiCS) Technology for Future Ultra High Density Memories.* 2013 International Symposium on Vlsi Technology, Systems, and Applications (Vlsi-Tsa), 2013.

40. Ichikawa, T., et al., *Topography simulation of BiCS memory hole etching modeled by elementary experiments of SiO(2) and Si etching.* Sispad 2010 - 15th

International Conference on Simulation of Semiconductor Processes and Devices, 2010: p. 45-48.

41. Shirota, R., *2 - Developments in 3D-NAND Flash technology*, in *Advances in Non-Volatile Memory and Storage Technology*, Y. Nishi, Editor. 2014, Woodhead Publishing. p. 27-74.

42. Fowler, R.H. and L. Nordheim, *Electron emission in intense electric fields.* Proceedings of the Royal Society of London Series a-Containing Papers of a Mathematical and Physical Character, 1928. **119**(781): p. 173-181.

43. Carey, J.D., R.D. Forrest, and S.R.P. Silva, *Origin of electric field enhancement in field emission from amorphous carbon thin films.* Applied Physics Letters, 2001. **78**(16): p. 2339-2341.

44. Fisher, J.C. and I. Giaever, *Tunneling through Thin Insulating Layers.* Journal of Applied Physics, 1961. **32**(2): p. 172-&.

45. Deheer, W.A., A. Chatelain, and D. Ugarte, *A Carbon Nanotube Field-Emission Electron Source.* Science, 1995. **270**(5239): p. 1179-1180.

46. Bonard, J.M., et al., *Field emission of individual carbon nanotubes in the scanning electron microscope.* Physical Review Letters, 2002. **89**(19).

47. Wu, Z.S., et al., *Field Emission of Single-Layer Graphene Films Prepared by Electrophoretic Deposition.* Advanced Materials, 2009. **21**(17): p. 1756-+.

48. Chen, I.C., S.E. Holland, and C.M. Hu, *Electrical Breakdown in Thin Gate and Tunneling Oxides.* Ieee Journal of Solid-State Circuits, 1985. **20**(1): p. 333-342.

49. Palnitkar, U.A., et al., *Remarkably low turn-on field emission in undoped, nitrogen-doped, and boron-doped graphene.* Applied Physics Letters, 2010. **97**(6).

50. Eda, G., et al., *Field emission from graphene based composite thin films.* Applied Physics Letters, 2008. **93**(23).

51. Malesevic, A., et al., *Field emission from vertically aligned few-layer graphene.* Journal of Applied Physics, 2008. **104**(8).

52. Meindl, J.D., et al., *Interconnect opportunities for gigascale integration.* IBM journal of research and development, 2002. **46**(2.3): p. 245-263.

53. Sarkar, J., *Chapter 1 - Sputtering Targets and Sputtered Films for the Microelectronic Industry*, in *Sputtering Materials for VLSI and Thin Film Devices*, J. Sarkar, Editor. 2014, William Andrew Publishing: Boston. p. 1-92.

54. Rossnagel, S.M. and T.S. Kuan, *Alteration of Cu conductivity in the size effect regime.* Journal of Vacuum Science & Technology B, 2004. **22**(1): p. 240-247.

55. Kimerling, L.C., *Photons to the rescue: Microelectronics becomes microphotonics.* The Electrochemical Society Interface, 2000. **9**(2): p. 28-31.

56. Samandari-Rad, J., M. Guthaus, and R. Hughey, *Confronting the Variability Issues Affecting the Performance of Next-Generation SRAM Design to Optimize and Predict the Speed and Yield.* Ieee Access, 2014. **2**: p. 577-601.

57. Vyas, A.A., C.J. Zhou, and C.Y. Yang, *On-Chip Interconnect Conductor Materials for End-of-Roadmap Technology Nodes.* Ieee Transactions on Nanotechnology, 2018. **17**(1): p. 4-10.

58. Tu, K.N., Y.X. Liu, and M.L. Li, *Effect of Joule heating and current crowding on electromigration in mobile technology.* Applied Physics Reviews, 2017. **4**(1).

59. Kim, K.S., et al., *Large-scale pattern growth of graphene films for stretchable transparent electrodes.* Nature, 2009. **457**(7230): p. 706-710.

60. Wang, M., et al., *A Platform for Large-Scale Graphene Electronics - CVD Growth of Single-Layer Graphene on CVD-Grown Hexagonal Boron Nitride.* Advanced Materials, 2013. **25**(19): p. 2746-2752.

61. Farmer, D.B., et al., *Utilization of a Buffered Dielectric to Achieve High Field-Effect Carrier Mobility in Graphene Transistors.* Nano Letters, 2009. **9**(12): p. 4474-4478.

62. Kondo, D., et al., *Low-Temperature Synthesis of Graphene and Fabrication of Top-Gated Field Effect Transistors without Using Transfer Processes.* Applied Physics Express, 2010. **3**(2).

63. Chen, J.H., et al., *Intrinsic and extrinsic performance limits of graphene devices on SiO2.* Nat Nanotechnol, 2008. **3**(4): p. 206-9.

64. Kumar, V., S. Rakheja, and A. Naeemi, *Performance and energy-per-bit modeling of multilayer graphene nanoribbon conductors.* Electron Devices, IEEE Transactions on, 2012. **59**(10): p. 2753-2761.

65. Kumar, V., S. Rakheja, and A. Naeemi, *Review of Multi-Layer Graphene Nanoribbons for on-chip Interconnect Applications.* 2013 Ieee International Symposium on Electromagnetic Compatibility (Emc), 2013: p. 528-533.

66. Wallace, P.R., *The Band Theory of Graphite.* Physical Review, 1947. **71**(9): p. 622-634.

67. Morgan, G.J. and C. Uher, *The C-axis electrical resistivity of highly oriented pyrolytic graphite.* Philosophical Magazine B, 1981. **44**(3): p. 427-430.

68. Kempa, H., P. Esquinazi, and Y. Kopelevich, *Field-induced metal-insulator transition in the c-axis resistivity of graphite.* Physical Review B, 2002. **65**(24).

69. Uher, C. and L.M. Sander, *Unusual temperature dependence of the resistivity of exfoliated graphites.* Physical Review B, 1983. **27**(2): p. 1326.

70. Habib, K.M.M., et al., *The coherent interlayer resistance of a single, rotated interface between two stacks of AB graphite.* Applied Physics Letters, 2013. **103**(24).

71. Kawamura, K., et al., *Electrical-Conduction in C-Direction of Highly Crystalline Graphites in Relation to Structural Perfection.* Journal of the Physical Society of Japan, 1979. **46**(2): p. 587-593.

72. Primak, W. and L.H. Fuchs, *Electrical Conductivities of Natural Graphite Crystals.* Physical Review, 1954. **95**(1): p. 22-30.

73. Sui, Y. and J. Appenzeller, *Screening and Interlayer Coupling in Multilayer Graphene Field-Effect Transistors.* Nano Letters, 2009. **9**(8): p. 2973-2977.

74. Aoki, M. and H. Amawashi, *Dependence of band structures on stacking and field in layered graphene.* Solid State Communications, 2007. **142**(3): p. 123-127.

75. Kim, Y., et al., *Breakdown of the Interlayer Coherence in Twisted Bilayer Graphene.* Physical Review Letters, 2013. **110**(9).

76. Santandrea, S., et al., *Field emission from single and few-layer graphene flakes.* Applied Physics Letters, 2011. **98**(16).

77. Chen, B.Y., et al., *How good can CVD-grown monolayer graphene be?* Nanoscale, 2014. **6**(24): p. 15255-15261.

78. Nashed, R., et al., *Ultra-High Mobility in Dielectrically Pinned CVD Graphene.* Ieee Journal of the Electron Devices Society, 2016. **4**(6): p. 466-472.

79. Zheng, Y., et al., *Gate-controlled nonvolatile graphene-ferroelectric memory.* Applied Physics Letters, 2009. **94**(16).

80. Standley, B., et al., *Graphene-Based Atomic-Scale Switches.* Nano Letters, 2008. **8**(10): p. 3345-3349.

81. Wang, X.M., et al., *Graphene/Metal Contacts: Bistable States and Novel Memory Devices.* Advanced Materials, 2012. **24**(19): p. 2614-2619.

82. Hwang, E.H., S. Adam, and S. Das Sarma, *Carrier transport in two-dimensional graphene layers.* Physical Review Letters, 2007. **98**(18).

83. Chen, J.H., et al., *Charged-impurity scattering in graphene.* Nature Physics, 2008. **4**(5): p. 377-381.

84. Ang, Y.S., et al., *Generalized Fowler-Nordheim field-induced vertical electron emission model for two-dimensional materials.* arXiv preprint arXiv:1711.05898, 2017.

85. Vasko, F.T. and I.V. Zozoulenko, *Conductivity of a graphene strip: Width and gate-voltage dependencies.* Applied Physics Letters, 2010. **97**(9).

86. Nishiyama, H. and M. Nakamura, *Capacitance of a Strip Capacitor.* Ieee Transactions on Components Hybrids and Manufacturing Technology, 1990. **13**(2): p. 417-423.

87. Silvestrov, P.G. and K.B. Efetov, *Charge accumulation at the boundaries of a graphene strip induced by a gate voltage: Electrostatic approach.* Physical Review B, 2008. **77**(15).

88. Ang, Y.S., S.J. Liang, and L.K. Ang, *Theoretical modeling of electron emission from graphene.* Mrs Bulletin, 2017. **42**(7): p. 506-510.

89. Zubair, M., Y.S. Ang, and L.K. Ang, *Fractional Fowler-Nordheim Law for Field Emission From Rough Surface With Nonparabolic Energy Dispersion.* Ieee Transactions on Electron Devices, 2018. **65**(6): p. 2089-2095.

90. Li, X.S., et al., *Large-Area Graphene Single Crystals Grown by Low-Pressure Chemical Vapor Deposition of Methane on Copper.* Journal of the American Chemical Society, 2011. **133**(9): p. 2816-2819.

91. Kim, W., et al., *Hysteresis caused by water molecules in carbon nanotube field-effect transistors.* Nano Letters, 2003. **3**(2): p. 193-198.

92. Prasad, N., et al., *Current induced annealing and electrical characterization of single layer graphene grown by chemical vapor deposition for future interconnects in VLSI circuits.* Applied Physics Letters, 2014. **105**(11).

93. Song, S.M., et al., *Determination of Work Function of Graphene under a Metal Electrode and Its Role in Contact Resistance.* Nano Letters, 2012. **12**(8): p. 3887-3892.

94. Mueller, T., et al., *Role of contacts in graphene transistors: A scanning photocurrent study.* Physical Review B, 2009. **79**(24).

95. Sinha, S., et al., *Exploring Sub-20nm FinFET Design with Predictive Technology Models.* 2012 49th Acm/Edac/Ieee Design Automation Conference (Dac), 2012: p. 283-288.

96. Reina, A., et al., *Large Area, Few-Layer Graphene Films on Arbitrary Substrates by Chemical Vapor Deposition.* Nano Letters, 2009. **9**(1): p. 30-35.

97. Reina, A., et al., *Large area, few-layer graphene films on arbitrary substrates by chemical vapor deposition.* Nano Lett, 2009. **9**(1): p. 30-5.

98. Lin, Y.-C., C.-Y. Lin, and P.-W. Chiu, *Controllable graphene N-doping with ammonia plasma.* Applied Physics Letters, 2010. **96**(13): p. 133110.

99. Estrada, D., et al., *Reduction of hysteresis for carbon nanotube mobility measurements using pulsed characterization.* Nanotechnology, 2010. **21**(8).

100. Venugopal, A., et al., *Effective mobility of single-layer graphene transistors as a function of channel dimensions.* Journal of Applied Physics, 2011. **109**(10).

101. Kim, S., et al., *Realization of a high mobility dual-gated graphene field-effect transistor with Al2O3 dielectric.* Applied Physics Letters, 2009. **94**(6).

102. Venugopal, A., L. Colombo, and E.M. Vogel, *Issues with characterizing transport properties of graphene field effect transistors.* Solid State Communications, 2012. **152**(15): p. 1311-1316.

103. Adam, S., et al., *A self-consistent theory for graphene transport.* Proceedings of the National Academy of Sciences of the United States of America, 2007. **104**(47): p. 18392-18397.

104. Ando, T., *Screening effect and impurity scattering in monolayer graphene.* Journal of the Physical Society of Japan, 2006. **75**(7).

105. Ponomarenko, L.A., et al., *Effect of a High-kappa Environment on Charge Carrier Mobility in Graphene.* Physical Review Letters, 2009. **102**(20).

106. Novikov, D.S., *Numbers of donors and acceptors from transport measurements in graphene.* Applied Physics Letters, 2007. **91**(10).

107. Bunch, J.S. and M.L. Dunn, *Adhesion mechanics of graphene membranes.* Solid State Communications, 2012. **152**(15): p. 1359-1364.

108. Ni, Z.H., et al., *Raman Spectroscopy and Imaging of Graphene.* Nano Research, 2008. **1**(4): p. 273-291.

109. Yuan, Q.H., G.Q. Yin, and Z.Y. Ning, *Effect of Oxygen Plasma on Low Dielectric Constant HSQ (Hydrogensilsesquioxane) Films.* Plasma Science & Technology, 2013. **15**(1): p. 86-88.

110. Jiao, L.Y., et al., *Facile synthesis of high-quality graphene nanoribbons.* Nature Nanotechnology, 2010. **5**(5): p. 321-325.

111. Eckmann, A., et al., *Probing the Nature of Defects in Graphene by Raman Spectroscopy.* Nano Letters, 2012. **12**(8): p. 3925-3930.

112. Cancado, L.G., et al., *Quantifying Defects in Graphene via Raman Spectroscopy at Different Excitation Energies.* Nano Letters, 2011. **11**(8): p. 3190-3196.

113. Ni, Z.H., et al., *Tunable stress and controlled thickness modification in graphene by annealing.* Acs Nano, 2008. **2**(5): p. 1033-1039.

114. Datta, S., *Quantum transport: atom to transistor*. 2005: Cambridge University Press.

115. Politou, M., et al., *Single-and multilayer graphene wires as alternative interconnects.* Microelectronic Engineering, 2016.

116. Tanachutiwat, S., et al. *Reconfigurable multi-function logic based on graphene pn junctions*. in *Design Automation Conference (DAC), .* 2010. IEEE.

117. Steinhogl, W., et al., *Comprehensive study of the resistivity of copper wires with lateral dimensions of 100 nm and smaller.* Journal of Applied Physics, 2005. **97**(2): p. 023706-023706-7.

118. International Technology Roadmap for Semiconductors (ITRS), available online at http://www.itrs.net/, 2012.

119. Pan, C., et al., *Technology/Circuit/System Co-Optimization and Benchmarking for Multilayer Graphene Interconnects at Sub-10-nm Technology Node.* Electron Devices, IEEE Transactions on, 2015. **PP**(99): p. 1-1.

120. Xia, F., et al., *The origins and limits of metal-graphene junction resistance.* Nature nanotechnology, 2011. **6**(3): p. 179-184.

121. Wang, X., et al., *Room-temperature all-semiconducting sub-10-nm graphene nanoribbon field-effect transistors.* Physical review letters, 2008. **100**(20): p. 206803.

122. Wang, L., et al., *One-Dimensional Electrical Contact to a Two-Dimensional Material.* Science, 2013. **342**(6158): p. 614-617.

123. Yue, D.W., et al., *Edge contacts of graphene formed by using a controlled plasma treatment.* Nanoscale, 2015. **7**(2): p. 825-831.

124. Verguts, K., et al., *Graphene delamination using 'electrochemical methods': an ion intercalation effect.* Nanoscale, 2018. **10**(12): p. 5515-5521.

125. Lu, C.C., et al., *Twisting Bilayer Graphene Superlattices.* Acs Nano, 2013. **7**(3): p. 2587-2594.

126. Carozo, V., et al., *Raman Signature of Graphene Superlattices.* Nano Letters, 2011. **11**(11): p. 4527-4534.

127. Jorio, A. and L.G. Cancado, *Raman spectroscopy of twisted bilayer graphene.* Solid State Communications, 2013. **175**: p. 3-12.

128. Campos-Delgado, J., et al., *Raman scattering study of the phonon dispersion in twisted bilayer graphene.* Nano Research, 2013. **6**(4): p. 269-274.

129. Kim, K., et al., *Raman Spectroscopy Study of Rotated Double-Layer Graphene: Misorientation-Angle Dependence of Electronic Structure.* Physical Review Letters, 2012. **108**(24).

130. Zhu, W., et al., *Carrier scattering, mobilities, and electrostatic potential in monolayer, bilayer, and trilayer graphene.* Physical Review B, 2009. **80**(23): p. 235402.

131. Partoens, B. and F.M. Peeters, *From graphene to graphite: Electronic structure around the K point.* Physical Review B, 2006. **74**(7).

132. Wu, X.Y., et al., *Boosting Carrier Mobility of Synthetic Few Layer Graphene on SiO2 by Interlayer Rotation and Decoupling.* Advanced Materials Interfaces, 2018. **5**(14).

133. Kempa, H., P. Esquinazi, and Y. Kopelevich, *Field-induced metal-insulator transition in the c-axis resistivity of graphite.* Physical Review B, 2002. **65**(24): p. 241101.

134. Bistritzer, R. and A.H. MacDonald, *Transport between twisted graphene layers.* Physical Review B, 2010. **81**(24).

135. Perebeinos, V., J. Tersoff, and P. Avouris, *Phonon-Mediated Interlayer Conductance in Twisted Graphene Bilayers.* Physical Review Letters, 2012. **109**(23).

136. Das, S. and J. Appenzeller, *Where Does the Current Flow in Two-Dimensional Layered Systems?* Nano Letters, 2013. **13**(7): p. 3396-3402.

137. Pan, C.Y., et al., *Technology/Circuit/System Co-Optimization and Benchmarking for Multilayer Graphene Interconnects at Sub-10-nm Technology Node.* Ieee Transactions on Electron Devices, 2015. **62**(5): p. 1530-1536.

138. LEE, H.J., E. Kim, and J. Jung. *Multi-Layer Graphene for High-Frequency Interconnect*. in *International Conference on Solid State Devices and Materials*. 2011 Nagoya, Japan.

139. Heo, K., et al. *Fabrication and Radio Frequency Characterization of Graphene Interconnect*. in *International Conference on Solid State Devices and Materials*. 2013. Fukuoka, Japan.

140. Nguyen, P.D., et al., *High frequency characterization of graphene nanoribbon interconnects.* Materials Research Express, 2014. **1**(3).

141. Cui, J.P., et al., *Signal Transmission Analysis of Multilayer Graphene Nano-Ribbon (MLGNR) Interconnects.* Ieee Transactions on Electromagnetic Compatibility, 2012. **54**(1): p. 126-132.

142. Kumar, V. and A. Naeemi, *Analytical Models for the Frequency Response of Multi-Layer Graphene Nanoribbon Interconnects.* 2012 Ieee International Symposium on Electromagnetic Compatibility (Emc), 2012: p. 440-445.

143. Kumar, V.R., et al., *Time and Frequency Domain Analysis of MLGNR Interconnects.* Ieee Transactions on Nanotechnology, 2015. **14**(3): p. 484-492.

144. Sarto, M.S. and A. Tamburrano, *Comparative Analysis of TL Models for Multilayer Graphene Nanoribbon and Multiwall Carbon Nanotube Interconnects.* 2010 Ieee International Symposium on Electromagnetic Compatibility (Emc 2010), 2010: p. 212-217.

145. Koolen, M.C.A.M., J.A.M. Geelen, and M.P.J.G. Versleijen, *An Improved De-Embedding Technique for on-Wafer High-Frequency Characterization.* Proceedings of the 1991 Bipolar Circuits and Technology Meeting, 1991: p. 188-191.